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METHOD 3131.4

*STEADY-STATE THERMAL IMPEDANCE AND TRANSIENT THERMAL IMPEDANCE TESTING OF TRANSISTORS
(DELTA BASE – EMITTER VOLTAGE METHOD)

* 1. Purpose. The purpose of this test is to determine the thermal performance of transistor devices. This can be done in two ways, steady-state thermal impedance or thermal transient testing. Steady-state thermal impedance (referred to as thermal resistance) determines the overall thermal performance of devices. A production-oriented screening process, referred to as transient thermal impedance testing, is a subset of steady-state thermal impedance testing and determines the ability of the transistor chip-to-header interface to transfer heat from the chip to the header, and is a measure of the thermal quality of the die attachment. It is relevant to designs which use headers, or heat conducting plugs, with mass and thermal conductivity allowing effective discrimination of poor die attachments. This is particularly true with power devices. The method can be applied to small signal, power, switching and Darlington transistors. This method is intended for production monitoring, incoming inspection, and pre-burn in screening applications. The measurement current (IM) must be large enough to ensure that the Darlington output transistor is biased into the linear conduction mode of the temperature sensing measurement periods of the thermal test.

* 1.1 Background and scope for transient thermal impedance testing. Transient thermal impedance of semiconductor devices are sensitive to the presence of voids in the die attachment material between the semiconductor chip and package since voids impede the flow of heat from the chip to the substrate (package). Due to the difference in the thermal time constants of the chip and package, the measurement of transient thermal impedance can be made more sensitive to the presence of voids than can the measurement of steady-state thermal impedance. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the package. Thus, the heating power pulse width can be selected so that only the chip and the chip-to-substrate interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant but less than that of the substrate. Heating power pulse widths ranging from 1 to 400 ms for various package designs have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heat sink the device under test (DUT). Thus, the transient thermal impedance techniques are less time consuming than the measurement of thermal resistance for use as a manufacturing screen, process control, or incoming inspection measure for die attachment integrity evaluation.

* 2. Definitions. The following symbols and terminology shall apply for the purpose of this test method:

a. V_{BE}: The forward biased base-emitter junction voltage of the DUT used for junction temperature sensing.

V_{BEi}: The initial V_{BE} value during application of measurement current (IM) and before application of heating power.

V_{BEf}: The final V_{BE} value during the sample window time (t_{SW}) after application and subsequent removal of heating power.

b. $\varnothing V_{BE}$: The change in, V_{BE}, (VBEi-VBEf) due to the application of heating power to the DUT.

c. I_H: The collector current applied to the DUT during the heating period.

d. V_{CE}: The voltage between the collector and emitter. V_{CE} is constant throughout the test.

e. P_H: The heating power applied the DFUT. $P_H = I_H \times V_{CE}$.

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f. t_H: The duration of the heating power pulse P_H.

g. ti: The time after application of the measurement current (IM) and before application of the heating power pulse.

h. I_M: The measurement current applied to forward bias the junction for measurement of V_{BE}.

i. t_{MD}: Measurement delay time is the time from the end of the heating power pulse to the beginning of the sample window time (t_{SW}). Delay must be sufficient in length to allow for attenuation of switching transients to occur. The delay time will vary according to the length of the cable to test fixture and associated fixture inductances.

j. t_{SW}: Sample window time during which final V_{BE} measurement is made. The value of t_{SW} should be small; and occur at precisely the conclusion of tMD. It can approach zero if an oscilloscope is used for manual measurements and no transient effects are present.

k. VTC: Voltage-temperature coefficient of V_{BE} with respect to T_J at a fixed value of I_M; in mV/ϒC.

l. K: Thermal calibration factor equal to the reciprocal of VTC; in ϒC/mV.

* m. CU: The comparison unit, consisting of $∅V_{BE}$ divided by V_{BE}, that is used to normalize the transient thermal impedance for variations in power dissipation; in units of mV/V.

n. T_J: The DUT junction temperature.

o. $∅T_J$: The change in T_J caused by the application of P_H for a time equal to t_H.

* p. $Z_{\theta JX}$: Transient. Thermal impedance from device junction to a time defined reference point; in units of ϒC/W.

* q. $Z_{\theta JC}$: Transient. Thermal impedance from device junction to a point on the outside surface of the case immediately adjacent to the device chip measured using time equal time constant of device; in units of ϒC/W.

* r. $R_{\theta JX}$: Steady-state. Thermal resistance from device junction to a defined reference point; in units of ϒC/W.

* s. $R_{\theta JC}$: Steady-state. Thermal resistance from device junction to a point on the outside surface of the case immediately adjacent to the device chip; in units of ϒC/W.

* t. $R_{\theta JA}$: Steady-state. Thermal resistance from device junction to an ambient (world); in units of ϒC/W.

u. TSP: The temperature sensitive parameter; V_{BE}.

3. Apparatus. The apparatus required for this test shall include the following, configured as shown on figure 3131-1, as applicable to the specified test procedure:

a. A constant current source capable of adjustment to the desired value of I_H and able to supply the V_{BE} value required by the DUT. The current source should be able to maintain the desired current to within ±2 percent during the entire length of heating time.

b. A constant current source to supply I_M with sufficient voltage compliance to turn the TSP junction fully on.

c. An electronic switch capable of switching between the heating period conditions and measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond or tens of microseconds range.

d. A voltage measurement circuit capable of accurately making the V_{BEf} measurement within the time frame with millivolt resolution.

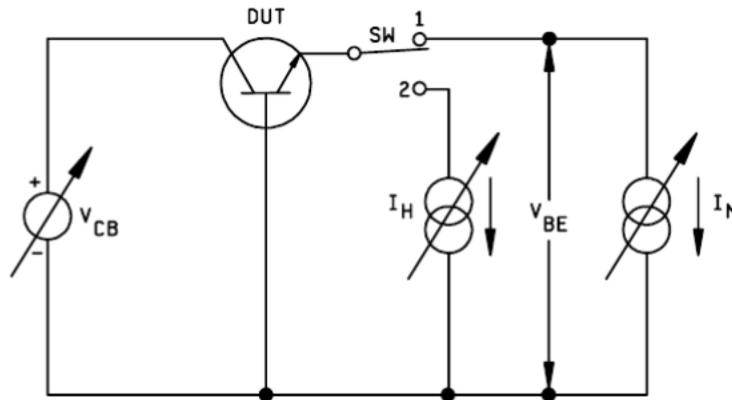

FIGURE 3131-1. Thermal impedance testing setup for transistors.

4. Test operation.

4.1 General description. The test begins with the adjustment of I_M and I_H to the desired values. The value of I_H is usually at least 50 times greater than the value of I_M. Then with the electronic switch in position 1, the value of V_{BEi} is measured. The switch is then moved to position 2 for a length of time equal to t_H and the value of V_{BE} is measured. Finally, at the conclusion of t_H, the switch is again moved to position 1 and the V_{BEf} value is measured within a time period defined by t_{MD} (or t_{MD} + t_{SW}, depending on the definitions stated previously). The two current sources are then turned off at the completion of the test.

4.2 Notes.

a. Some test equipment may provide a $\varnothing VBE$ directly instead of V_{BEi} and V_{BEf}; this is an acceptable alternative. Record the value of $\varnothing V_{BE}$.

b. Some test equipment may provide $Z_{\theta JX}$ directly instead of V_{BEi} and V_{BEf} for thermal resistance calculations; this is an acceptable alternative. Record the value of $Z_{\theta JX}$.

c. Alternative waveforms, as may be generated by ATE using the general principles of this method, may be used upon approval of the qualifying activity.

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5. Acceptance limit.

5.1 General discussion. Variations in transistor characteristics from one manufacturer to another cause difficulty in establishing a single acceptance limit for all transistors tested to a given specification. Ideally, a single acceptance limit value for ØV_{BE} would be the simplest approach. However, different design, materials, and processes can alter the resultant ØV_{BE} value for a given set of test conditions. Listed below are several different approaches to defining acceptance limits. The ØV_{BE} limit is the simplest approach and is usually selected for screening purposes. Paragraphs 5.3 through 5.6 require increasingly greater detail or effort.

5.2 ØV_{BE} limit. A single ØV_{BE} limit is practical if the K factor and V_{BE} values for all transistors tested to a given specification are nearly identical. Since these values may be different for different manufacturers, the use of different limits is likely to more accurately achieve the desired intent. (A lower limit does not indicate a better die bond when comparing different product sources.) The transistor specifications would list the following test conditions and measurement parameters:

a. I_H (in A).

b. t_H (in ms).

c. I_M (in mA).

d. t_{MD} (in ∝s).

e. t_{SW} (in ∝s).

f. ØV_{BE} (maximum limit value, in mV).

5.3 ØT_J limit. (Much more involved than ØVBE , but useful for examining questionable devices.) Since ØT_J is the product of K (in accordance with 6.) and ØV_{BE}, this approach is the same as defining a maximum acceptable junction temperature rise for a given set of test conditions.

5.4 CU limit. (Slightly more involved than ØT_J.) The ØT_J limit approach described above does not take into account potential power dissipation variations between devices. The V_{BE} value can vary, depending on chip design and size, thus causing the power dissipation during the heating time to be different from device to device. This variation will be small within a lot of devices produced by a single manufacturer but may be large between manufacturers. A CU limit value takes into account variations in power dissipation due to differences in V_{BE} by dividing the ØV_{BE} value by V_{BE}.

5.5 (K∝CU) limit. (Slightly more involved but provides greater detail.) This is a combinational approach that takes into account both K factor and power dissipation variations between devices.

* 5.6 $Z_{\theta JX}$ limit. (For full characterization; not required for screening purposes, but preferred if the proper ATE is available.) The transient thermal impedance approach uses an absolute magnitude value specification that overcomes the problems associated with the other approaches. transient Thermal impedance is time dependent and is calculated as follows:

$$Z_{\Theta JX} = \frac{\varnothing T_J}{P_D} = \left| \frac{(K)(\varnothing V_{BE})}{(I_H)(V_H)} \right| {}^{o}\text{C/W}$$

5.7 $R_{\theta JX}$ limit. (For thermal resistance specification testing.) The thermal resistance to some defined point, such as the case, is an absolute magnitude value specification used for equilibrium conditions. The t_H heating time must therefore be extended to appreciably longer times (typically 20 to 50 seconds). In the example of $R_{\theta JC}$ measurements, the case must be carefully stabilized and monitored in temperature which requires an infinite heat sink for optimum results. The $\varnothing T_J$ is the difference in junction temperature to the case temperature for the example of $R_{\theta JC}$.

$$R_{\Theta JX} = \frac{\varnothing T_J}{P_D} = \left| \frac{(K)(\varnothing V_{BE})}{(I_H)(V_H)} \right| {}^{o}\text{C/W}$$

* 5.8 General comment for transient thermal impedance testing. One potential problem in using the transient thermal impedance testing approach lies in trying to make accurate enough measurements with sufficient resolution to distinguish between acceptable and nonacceptable transistors. As the DUT current handling capability increases, the thermal impedance under transient conditions will become a very small value. This raises the potential for rejecting good devices and accepting bad ones. Higher I_H values must be used in this case.

6. Measurement of the TSP V_{BE}. The calibration of V_{BE} versus T_J is accomplished by monitoring V_{BE} for the required value of I_M as the environmental temperature (and thus the DUT temperature), and is varied by external heating. It is not required if the acceptance limit is $\varnothing V_{BE}$ (see 5.2), but is relevant to the other acceptance criteria (see 5.3 through 5.6). The magnitude of I_M shall be chosen so that V_{BE} is a linearly decreasing function over the normal T_J range of the device. I_M must be large enough to ensure that the base-emitter junction is turned on but not large enough to cause significant self-heating. An example of the measurement method and resulting calibration curve is shown on figure 3131-2.

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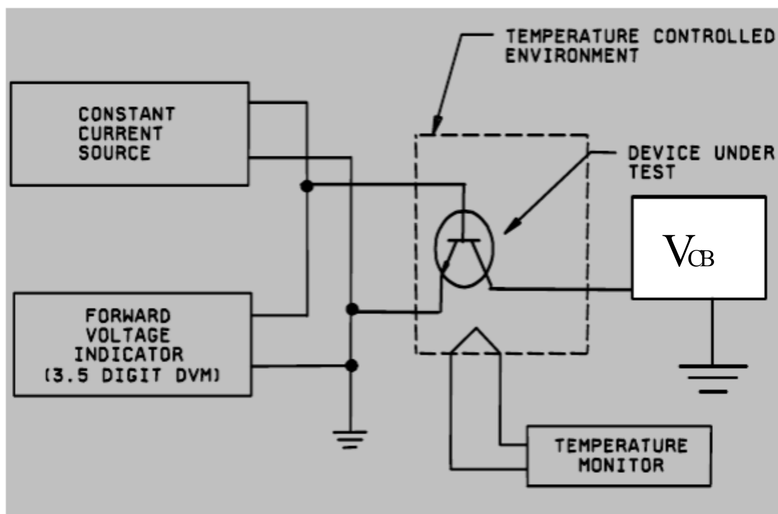
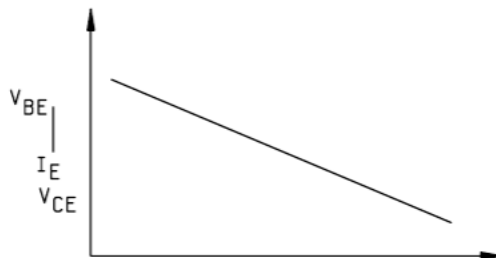


Step 1: Measure V_{BE1} at T_{J1} using I_M
Step 2: Measure V_{BE2} at T_{J2} using I_M

Step 3: $K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| °C/mV$



I_M: Must be large enough to overcome surface leakage effects but small enough not to cause significant self-heating.

T_J: Is externally applied (e.g., via oven, liquid) environment.

FIGURE 3131-2. Example curve of V_{BE} versus T_J.

A calibration factor K (which is the reciprocal of the slope of the curve on figure 3131-2) can be defined as:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| \ ^\circ C/mV$$

The K factor is used to calibrate the DUT such that the measured forward voltage drop corresponds to the temperature of the junction at a given bias condition. In order to ensure accurate results, the bias conditions used to determine the K factor must be chosen such that the application is duplicated. Therefore, the results will be unique for each particular biasing condition and should be reestablished for different values of base and/or collector currents (IF for diodes). This method should be used for each of the following conditions: Transient thermal impedance, burn-in, and life tests. Verify actual TJ seen by a device in field applications.

It has been found experimentally that the K-factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 piece to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than three percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in determining device acceptance. As an alternative to using individual values of K, the manufacture may establish internal limits unique to their product that ensures atypical product removal from the population (lot-to-lot and within-the-lot). The manufacturer shall use statistic techniques to establish the limits to the satisfaction of the government.

7. Establishment of test conditions and acceptance limits. Thermal resistance measurements require that I_H be equal to the required value stated in the device specifications, typically at rated current or higher. Values for t_H, t_{MD}, and heat sink conditions are also taken from the device specifications. The steps shown below are primarily for transient thermal impedance testing and thermal characterization purposes.

The following steps describe how to set up the test conditions and determine the acceptance limits for implementing the transient thermal test for die attachment evaluation using the apparatus and definitions stated above.

7.1 Initial device testing procedure. The following steps describe in detail how to set up the apparatus described previously for proper testing of various transistors. Since this procedure thermally characterizes the transistor out to a point in heating time required to ensure heat propagation into the case (i.e., the $R_{\theta JX}$ condition), an appropriate heat sink should be used or the case temperature should be monitored.

* Step 1: From a 20 to 25 piece sample, pick any one diode to start the setup process. Set up the test apparatus as follows:

I_H = 1.0 A (Or some other desired value near the DUTs normal operating current, typically higher for power transistors.

t_H = 10-50 ms Unless otherwise specified, for most devices rated up to 15 W power dissipation.

50 - 100 ms Unless otherwise specified, for most devices rated up to 200 W power dissipation.

* ≥ 250 ms For steady-state thermal impedance measurement. The pulse must be shown to correlate to steady-state conditions before it can be substituted for steady-state condition.

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t_{MD} = 100 ∝s max A larger value may be required on power devices with inductive package elements which generate nonthermal electrical transients; unless otherwise specified, this would be observed in the t_3 region of figure 3131-3.

I_M = 10 mA (Or some nominal value approximately two percent, or less, of I_H.)

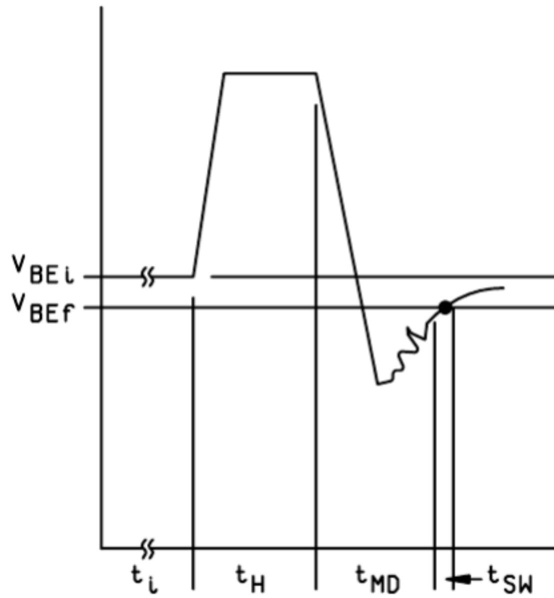

FIGURE 3131-3. Thermal impedance testing waveforms.

Step 2: Insert device into the apparatus test fixture and initiate a test. (For best results, a test fixture that offers some form of heat sinking would be desirable. Heat sinking is not needed if either the power dissipation during the test is well within the diode's free-air rating or the maximum heating time is limited to less than that required for the heat to propagate through the case.)

Step 3: If ΔV_{BE} is in the 15 to 80 mV range then proceed to the next step. This range approximately corresponds to a junction temperature change of roughly +10°C to +50°C and is sufficient for initial comparison purposes.

If ΔV_{BE} is less than 15 mV, return to 7.1, step 1 and increase heating power into device by increasing I_H.

If ΔV_{BE} is greater than 80 mV, approximately corresponding to a junction temperature change greater than +50°C, it would be desirable to reduce the heating power by returning to 7.1, step 1 and reducing I_H.

NOTE: The test equipment shall be capable of resolving ΔV_{BE} to within five percent. If not, the higher value of ΔV_{BE} must be selected until the five percent tolerance is met. Two different devices can have the same junction temperature rise even when P_H is different, due to widely differing V_{BE}. Within a given lot, however, a higher V_{BE} is more likely to result in a higher junction temperature rise. For such examples, this screen can be more accurately accomplished using the CU value. As defined in 2m., CU provides a comparison unit that takes into account different device V_{BE} values for a given I_H test condition.

Step 4: Test each of the sample devices and record the data detailed in 8.1.

Step 5: Select out the devices with the highest and lowest values of CU or $Z_{\theta JX}$ and put the remaining devices aside.

The ΔV_{BE} values can be used instead of CU or $Z_{\theta JX}$ if the measured values of V_{BE} are very tightly grouped around the average value.

Step 6: Using the devices from 7.1, step 5, collect and plot the heating curve data for the two devices in a manner similar to the examples shown on figure 3131-4.

Step 7: Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical chips should be the same if the heating time (t_H) is less than or equal to the thermal time constant of the chip, the two curves should start out the same for the low values of t_H. Non-identical chips (thinner or smaller in cross section) will have completely different curves, even at the smaller values of t_H. As the value of t_H is increased, thereby exceeding the chip thermal constant, heat will have propagated through the chip into the die attachment region. Since the heating curve devices of 7.1, step 5 were specifically chosen for their difference, the curves of figure 3131-4 diverge after t_H reaches a value where the die attachment variance has an affect on the device junction temperature. Increasing t_H further will probably result in a flattening of the curve as the heating propagates in the device package. If the device package has little thermal mass and is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope.

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Step 8: Using the heating curve, select the appropriate value of t_H to correspond to the inflection point in the transition region between heat in the chip and heat in the package.

If there are several different elements in the heat flow path: Chip, die attachment, substrate, substrate attach, and package, for example in a hybrid, there will be several plateaus and transitions in the heating curve. Appropriate selection of t_H will optimize evaluation sensitivity to other attachment areas.

Step 9: Return to the apparatus and set t_H equal to the value determined from 7.1, step 8.

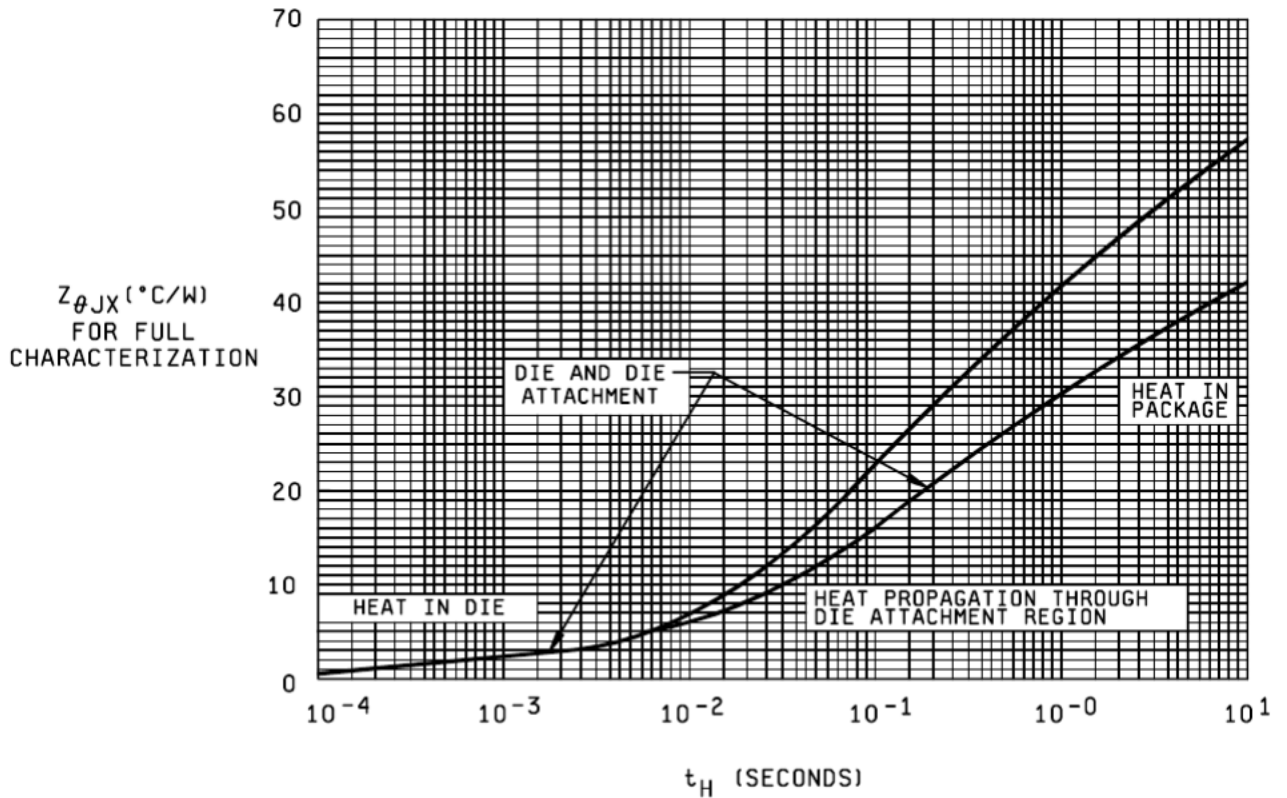

FIGURE 3131-4. Heating curves for two extreme devices.

Step 10: Because the selected value of t_H is much less than that for thermal equilibrium, it is possible to significantly increase the heating power without degrading or destroying the device. The increased power dissipation within the DUT will result in higher $\varnothing V_{BE}$ or CU values that will make determination of acceptable and nonacceptable devices much easier.

Step 11: The pass/fail limit, the cut-off point between acceptable and nonacceptable devices, can be established in a variety of ways:

a. Correlation to other die attachment evaluation methods, such as die shear and x-ray, while these two methods have little actual value from a thermal point of view, they do represent standardization methods as described in various military standards.

b. Maximum allowable junction temperature variations between devices, since the relationship between $\varnothing T_J$ and $\varnothing V_{BE}$ is about 0.5ΥC/mV for forward bias testing, or 0.25C/mV for Darlington transistors, the junction temperature spread between devices can be easily determined. The T_J predicts reliability. Conversely, the T_J spread necessary to meet the reliability projections can be translated to a $\varnothing V_{BE}$ or CU value for pass/fail criteria.

To fully utilize this approach, it will be necessary to calibrate the devices for the exact value of the T_J to V_{BE} characteristic. The characteristic's slope, commonly referred to as K factor, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature indicator, and a power supply setup as described in 6. A simple set of equations yield the junction temperature once K and $\varnothing V_{BE}$ are known:

$\varnothing T_J = (K)(\varnothing VBE)$

$T_J = T_A + \varnothing T_J$

Where: T_A is the ambient or reference temperature. For thermal transient test conditions, this temperature is usually equivalent to case temperature (T_C) for case mounted devices.

c. Statistically from a 20 to 25 device sample, the distribution of $\varnothing V_{BE}$ or CU values should be a normal one with defective devices out of the normal range. Figure 3131-5 shows a $\varnothing V_{BE}$ distribution for a sample lot of transistors. NOTE: The left-hand side of the histogram envelope is fairly well defined but the other side is greatly skewed to the right. This comes about because the left-hand side is constrained by the absolutely best heat flow that can be obtained with a given chip assembly material and process unless a test method error is introduced. The other side has no such constraints because there is no limit as to how poorly a chip is mounted.

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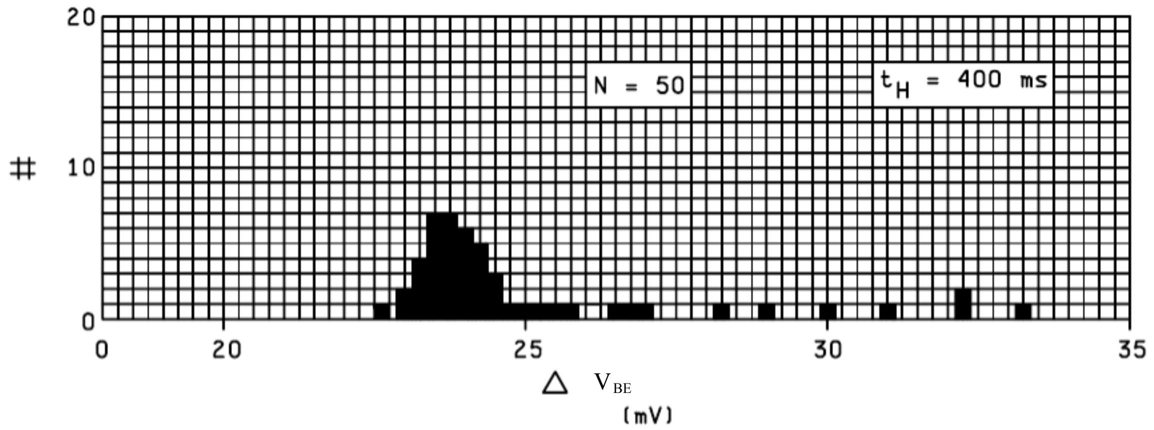

FIGURE 3131-5. Typical ∅V_{BE} distribution

The usual rule of thumb in setting the maximum limit for ∅V_{BE} , CU, or $Z_{\theta JX}$ is to use the distribution average value and three standard deviations (σ). For example:

$| (\varnothing V_{BE}) | = \overline{\varnothing V_{BE}} + X\sigma$

high
limit

$| (CU) | = \overline{CU} + X\sigma$

high
limit

$| (Z_{\theta JX}) | = \overline{Z_{\theta JX}} + X\sigma$

high
limit

Where: X = 3 in most cases and $\overline{\varnothing V_{BE}}$, $\overline{\varnothing CU}$, and $\overline{\varnothing Z_{\theta JX}}$ are the average distribution values.

The statistical data required is obtained by testing 25 or more devices under the conditions of 7.1, step 11.

The maximum limit determined from this approach should be correlated to the transistor's specified thermal resistance. This will ensure that the ∅V_{BE} or CU limits do not pass diodes that would fail the thermal resistance or transient thermal impedance requirements.

Step 12: Once the test conditions and pass/fail limit have been determined, it is necessary only to record this information for future testing requirements of the same device in the same package. It is also recommended that a minimum limit is established to ensure a test method error or other anomaly is investigated.

Step 13: After the pass/fail limits are established, there shall be verification they correllate to good and bad bonded devices or the electrical properties such as surge.

The steps listed hereto are conveniently summarized in table 3131-I.

TABLE 3131-I. Summary of test procedure steps.

General description		Steps	Comments
A	Initial setup	1 through 4	Approximate instrument settings to find variations among devices in 10 to 15 piece sample.
B	Heating curve generation	5 through 6	Using highest and lowest reading devices, generate heating curves.
C	Heating curve interpretation	7 through 9	Heating curve is used to find more appropriate value for t_H corresponding to heat in the die attachment area (for some other desired interface in the heat flow path).
D	Final setup	10	Heating power applied during t_H is increased in order to improve measurement sensitivity to variations among devices.
E	Pass-fail determination	11 through 12	A variety of methods is available such as JESD 34 for setting the fail limit; the statistical approach is the fastest and easiest to implement.
F	Verification	13	Mechanical / Electrical correlation

7.2 Routine device thermal transient testing procedure. Once the proper control settings have been determined for a particular device type from a given manufacturing process or vendor, repeated testing of that device type simply requires that the same test conditions be used as previously determined. New device types or the same devices manufactured with a different process will require a repeat of 7.1 for proper thermal transient test conditions.

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8. Test conditions and measurements to be specified and recorded.

* 8.1 Transient thermal impedance-steady-state thermal impedance measurements.

8.1.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___ mA

b. I_H heating current ___ A

c. t_H heating time ___ ms

d. t_{MD} measurement time delay ___∝s

e. t_{SW} sample window time ___ ∝s

8.1.2 Data. Record the following data:

a. V_{BEi} initial forward voltage ___V

b. V_H heating voltage ___V

c. V_{BEf} final forward voltage ___V

(NOTE: Some test equipment may provide a ∅V_{BE} instead of V_{BEi} and V_{BEf}, this is an acceptable alternative. Record the value of ∅V_{BE}.

Some test equipment may provide direct display of calculated CU or $Z_{\theta JX}$; this is an acceptable alternative. Record the value of CU or $Z_{\theta JX}$.

8.2 K factor calibration. (Optional for criteria 8.3a or 8.3b, mandatory for 8.3c, 8.3d, or 8.3e.)

8.3 Test conditions. Specify the following test conditions:

a. I_M current magnitude ___mA

b. Initial junction temperature ___ϒC

c. Initial V_{BE} voltage ___mV

d. Final junction temperature ___ϒC

e. Final V_{BE} voltage ___mV

8.4 K factor. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{BE2} - V_{BE1}} \right| ϒ C/mV$$

K factor ___ϒC/mV

8.5 Specification limit calculations. One or more of the following should be measured or calculated, as called for on the device specification (see 5.1):

∅V_{BE}	___mV
CU	___mV/V
∅T_J	___ϒC
K∝CU	___ϒC/V
$Z_{\theta JX}$	___ϒC/W
$R_{\theta JX}$	___ϒC/W

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