JEDEC STANDARD

Test Boards for Area Array Surface Mount Package Thermal Measurements

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Electronic Industries Alliance

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TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL MEASUREMENTS

CONTENTS

Foreword

Previous thermal test board standards for leaded surface mount components have described the need for a standardized thermal test board design to allow comparison of thermal test results between organizations [1-2]. The present standard describes design standards for a test board that will allow no more than 15% measurement variability to occur between the minimum and maximum design parameters of the specification. The standard is not intended to give actual in-use values, but rather a figure of merit for use in comparing packages. Reference to the board used, 2s (1s effective) or 2s2p, must be made for all reported results.

This specification is intended for use with the thermal measurements and modeling specifications grouped under the JEDEC EIA/JESD51 series, [1]. Specifically, the electrical test procedures described in JEDEC EIA/JESD51-1, “Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device),” [2], EIA/JESD51-2, “Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air) ”, [3], and EIA/JESD51-6, “Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air) ”, [4].

TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL MEASUREMENTS

(From JEDEC Board Ballot JCB-00-14, formulated under the cognizance of the JC-15.1 Subcommittee on Thermal Characterization.)

1 Scope

This specification is meant to be broad enough to incorporate a wide variety of surface mount area array package (e.g., BGA) design features and technologies. However, due to a limited number of signal layers that results in shorting some device pins in this specification, the boards described here may not be adequate for measurement of active devices as compared to applications with thermal test chips.

This specification covers surface mount area array packages intended to be mounted on a PCB. It does not cover area array packages that require sockets or PGA packages.

2 Normative references

The following standards contain provisions that, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

[1] EIA/JESD51, *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)*.

[2] EIA/JESD51-1, *Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device)*.

[3] EIA/JESD51-2, *Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*.

[4] EIA/JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*.

[5] *Electronics Engineer's Handbook*, 3rd Edition, Edited by D.G. Fink and D. Christiansen, McGraw-Hill Book Co., NY, 1989, p 6.16

[6] MIL-W-5088L, Amdt.1, *Wiring, Areospace Vehicle.*

3 Stock material

The PCB test board shall be made of FR-4 material. The finish size shall be 1.60 mm +/- 10% thick. For high ambient or board temperature applications (> 125 ºC), use of other test board material is acceptable as long as the thermal conductivity of the material is reported and measurement correlations have been established between the substitute material and FR-4.

Trace thicknesses are achieved by starting with standard copper stock and then plating to final thicknesses. A convention in PCB fabrication is to refer to copper thickness using the terminology ounces of copper per square foot of board. An ounce of copper per square foot translates to a copper thickness of 35 ∝m.

The 1s test board has only a top trace layer in the component mounting and trace fan-out region (see figure 1a). The copper trace thickness shall be 70 ∝m (2 oz) +/- 20% for a ball pitch of > 0.5 mm and 50 ∝m (1.5 oz) +/- 20% for a ball pitch ″ 0.5 mm. A bottom trace layer may be used for solder lands at the end of the fan-out traces and edge connection points. Connection to the edge connector outside the package fan-out region can be made with either the top or bottom signal traces. The 2s2p version of this test board is formed by embedding two 35 ∝m (1 oz) +0/-20% copper planes in the PCB (as shown in figure 1b), while maintaining the finish thickness at 1.60 mm.

Figure 1a — Cross section of 1s PCB showing trace and dielectric thicknesses in package placement and trace fan-out regions

Figure 1b — Cross section of 2s2p PCB showing trace and dielectric thicknesses

4 Board outline

The board shall be 101.5 mm x 114.5 mm +/- 0.25 mm in size for packages less than or equal to 40 mm on a side (see figure 2). A typical edge connector is depicted in figure 2. The edge connector can be pin-out and pitch modified for specific needs. Modification of the width dimension of the edge connector is allowed. Multiple rows of vias along the edge connector are allowed.

For various package sizes, refer to table 1 for the appropriate PCB size.

Table 1 — PCB sizes for packages

Package Length	PCB Size (+/- 0.25 mm)
Pkg. Length ″ 40 mm	101.5 mm x 114.5 mm (4.0 in x 4.5in)
40 mm < Pkg. Length ″ 65 mm	127.0 mm x 139.5 mm (5.0 in x 5.5 in)
65 mm < Pkg. Length ″ 90 mm	152.5 mm x 165.0 mm (6.0 in x 6.5 in)

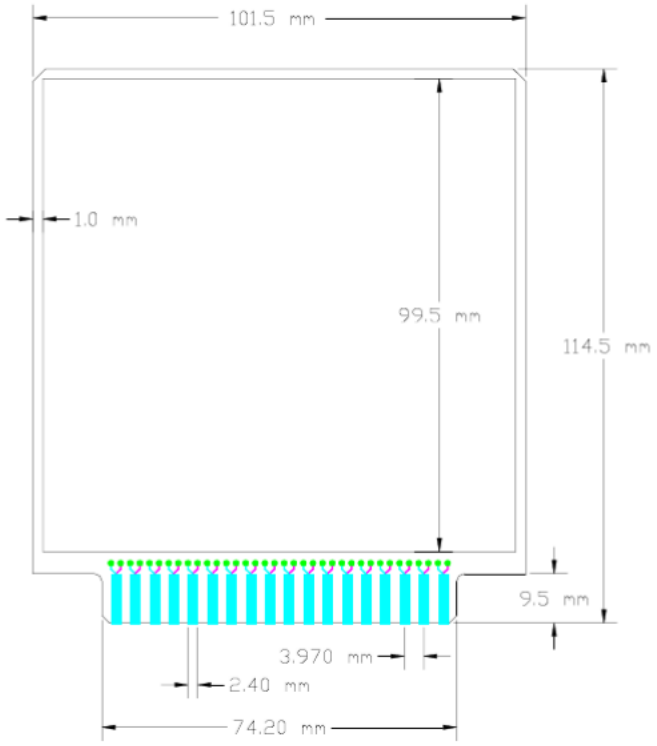


Figure 2 — BGA test board outer dimensions and edge connector design.

5 Trace design

5.1 Top trace layer layout (both 1s and 2s2p PCBs)

Traces shall be laid out such that the test device will be centered relative to a 101.5 mm x 101.5 mm section towards the top of the board (away from the edge connector) for the smallest board. For larger board sizes, locate the package at the top of the board in the center of a square whose length is the width dimension of the board. The traces connecting to the package must extend at least 25 mm out from the edge of the device body. Trace lengths longer than this amount are allowed. Traces must be routed in a radial fashion (flared) to meet the edges of a square such that the terminal via locations are equally spaced over 90% of the perimeter of the sides of this square. Lands must be flared out to the 25 mm perimeter adjacent to the side of the package they are on. Corner-most lands flare to the perimeter clockwise of the corner (see figures 3 & 4). Staggering of trace terminal soldering positions inward from the trace termination square is allowed to 2.5 mm off the perimeter of the square.

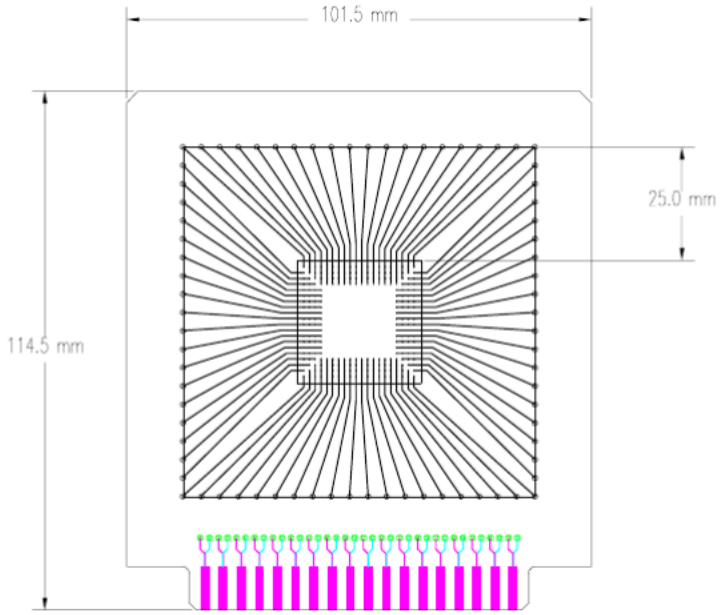


Figure 3 — Traces to outer ball row flared to perimeter 25 mm from package body.

5 Trace design (cont'd)

5.1 Top trace layer layout (both 1s and 2s2p PCBs) (cont'd)

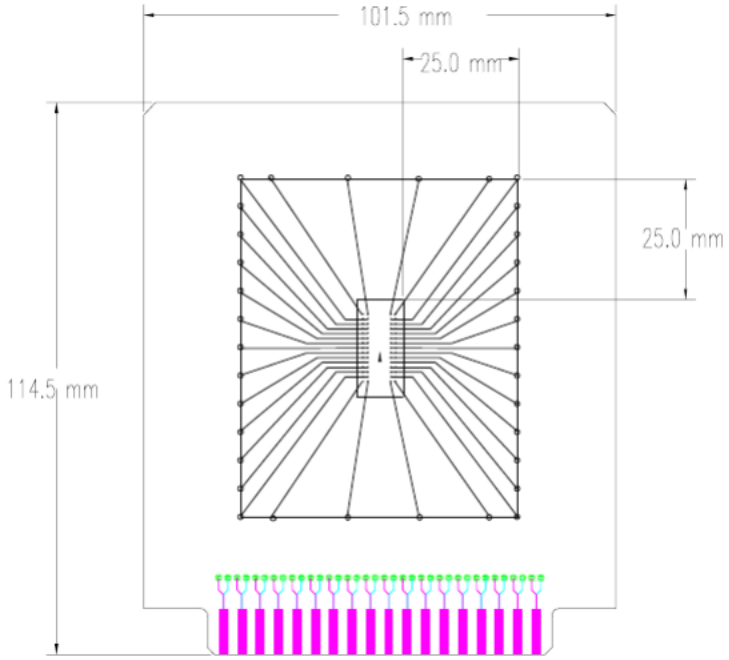


Figure 4 — Flared PCB layout scheme. Traces flared to meet via holes.

Traces must short all ball rows on a given side of a package together as shown in figure 5. If the package interposer is designed so that two connections needed for the thermal test would be shorted when the ball rows are shorted together, the trace may be cut to eliminate the short (see figure 5). No more than 10% of the total number of traces should be cut. Routing two traces between balls is allowed for interconnect of signal or power to the same column of balls (as shown in figure 5g) as long as the total trace width per ball position in the fan-out region is as specified in 5.3. The routing of figure 5g may require the use of traces that are narrower than specified in 5.3 in the ball array area. This is allowed as long as the portion of the trace outside the package body is in agreement with the width specified in 5.3. A trace design that nests packages with equal ball pitches on the same PCB is allowed as long as the above conditions are met (see figure 6).

1s design only: For packages with partial ball arrays, traces must be routed towards the center of the package as if the package had a full matrix ball array as shown in figure 5a and 5c. This will minimize measurement variation from PCB design for cases when package underfill is used.

5 Trace design (cont'd)

5.2 Traces to thermal balls

1s design: Lands for a center array of package thermal balls must be routed out to the external trace fan-out pattern as shown in either figure 5e, 5f, or 5g. Variation of this pattern is allowed to ensure V_{HI} and V_{LO} thermal balls are routed to appropriate external traces. A thermal ball is a ball associated with a thermal via in a center array of balls on the package that are primarily intended to provide heat transport from the chip to the board. All thermal balls in a center array must be shorted to traces that route to the external trace fan-out pattern. If an underfill is used between the package and the test board and the package has no thermal balls, the traces to the center array of thermal ball lands must be cut between the signal ball land array and the thermal ball land array.

2s2p design: Trace connections are not allowed from the trace fan-out pattern on the outer signal balls to the thermal ball pattern (e.g., figure 5h). Connection of the thermal balls on a 2s2p board design is only allowed to thermal vias, which then connect to the top buried plane as described in 5.5.

5.3 Trace widths for 1s and 2s2p PCBs

Finished trace widths shall be from 36% to 44% of the package solder ball pitch for one trace per ball position designs (see figure 5a-5f). For example, a package with a 1.0 mm pitch should have a finished trace width of 0.40 mm +/- 0.04 mm. For two trace per ball position designs (figure 5g), the total finished trace width shall be from 36% to 44% of the solder ball pitch for pitches > 0.5 mm. For pitches ″ 0.5 mm., the total finished trace width shall be 45% to 55% of the solder ball pitch. Achieving the finish size may require some oversize in design to compensate for over-etching of the copper traces during processing. Traces shall terminate in a plated through-hole for soldering interconnect purposes. See 5.10 for a description of the plated through-hole vias.

5 Trace design (cont'd)

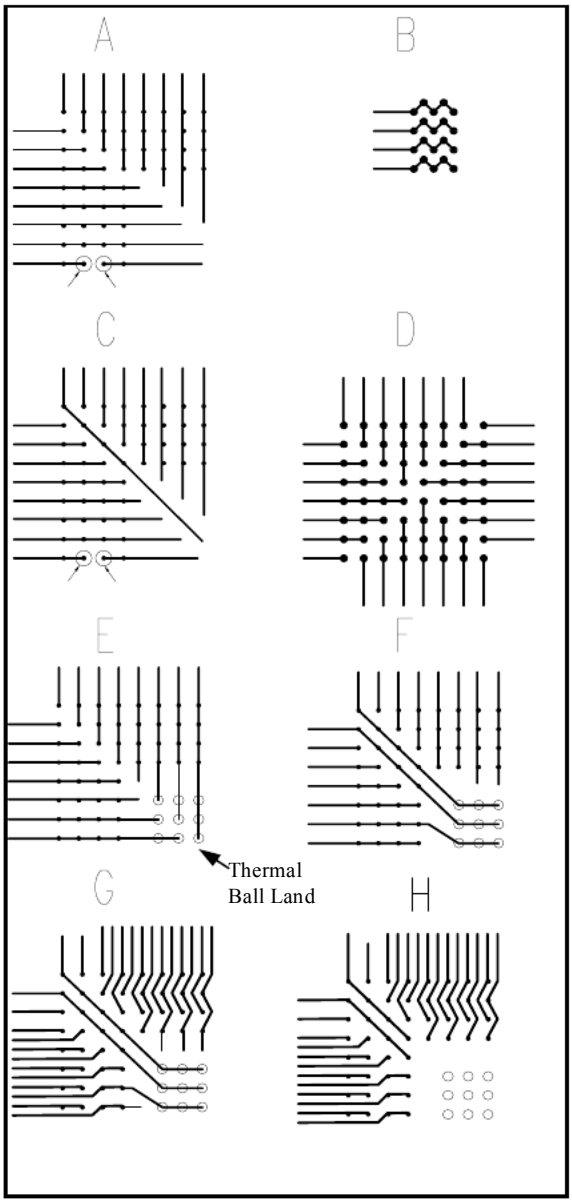


Figure 5 — Package footprint routing

Examples:

a) Routing a corner of an array - arrows highlight a trace broken to eliminate a V_{HI} to V_{LO} short
b) Routing a staggered array
c) Routing with a diagonal corner trace
d) Full array routing schematic
e) Routing to thermal balls (open circles) at center of package (1s only)
f) Routing to thermal balls using diagonal connections (1s only)
g) 2 traces per ball position routing options. Total trace width to be 40% of ball pitch for each ball position. Top of diagram shows connection of every other ball. Side of diagram shows connection of every other ball pair. Center connection to thermal balls for 1s design only.
h) No connection allowed to thermal balls on 2s2p design

5 Trace design (cont'd)

5.4 Ball lands for 1s and 2s2p PCBs

Ball lands should be sized according to the technology in use for the solder balls. Solder masking must be used to avoid solder wicking from the ball into through-hole vias on the thermal test board or onto electrical interconnect traces.

5.5 Thermal ball lands and thermal vias

1s PCB: Thermal vias in the 1s PCB are not allowed.

2s2p PCB: All center thermal balls on the package shall connect to the top buried copper plane through thermal vias on the test PCB. This plane may be either the buried V_{HI} or V_{LO}. The thermal vias shall have drill diameters as specified in table 2 as a function of the ball pitch of the package and shall be plated to 18 ∝m copper minimum thickness throughout the via barrel. A cross pattern on the connected plane shall not be used; the connected plane shall remain unetched in the vicinity of the drill hole. When isolating a thermal via from a buried plane, use an isolation clearance diameter no less than 0.20 mm greater than the hole diameter. The isolation clearance regions for adjacent thermal vias shall not merge, making the buried plane discontinuous. The thermal via must be offset from the ball land to avoid wicking the solder ball into the via during solder reflow.

Table 2 — Drill diameters for thermal vias vs. ball pitch

Ball pitch	Thermal via outer diameter (O.D.)
1.50 mm	0.40 mm +/- 10%
1.27 mm	0.35 mm +/- 10%
1.00 mm	0.30 mm +/- 10%
0.75 mm – 0.80 mm	0.25 mm +/- 10%
0.65 mm	0.20 mm +/- 10%
0.50 mm	0.20 mm +/- 10%

To allow for nesting of different packages on the same PCB design, the thermal ball lands may be arrayed to match the largest thermal ball array of the packages to be tested on the PCB. If a thermal ball land and via pair in such an array are actually being used by a signal I/O, the connection between the thermal ball land and via may be cut or trimmed without violating this specification. Such trimming should remove as much of the connecting trace as possible.

5 Trace design (cont'd)

5.6 Trace layers and connection routing

1s PCB: The only pattern permitted within the flared perimeter (fan-out area) is the fan-out pattern and package footprint on the top trace layer. The bottom layer shall be used only for via termination and limited connection routing to the edge connector. Routing to the edge connector is allowed in either the top or bottom signal layers if the interconnection remains outside the flared perimeter of the through holes (see figure 7). No traces, except as noted below, are allowed to run under the PCB within the flared perimeter of the through holes. Power connection routing should be designed to minimize voltage drops and self-heating across the PCB traces. Measurement force (power) and sense (measure) lines should be kept independent of each other from the edge connector to the package terminals.

2s2p PCB: The top trace layer shall be used for fan-out and interconnection to the edge connector outside the fan-out perimeter. Any required interconnection routing to the edge connector can be made using the bottom trace layer and the top layer as long as the top layer interconnection remains outside the package fan-out region. Power connection routing should be designed to minimize voltage drops and self-heating across the PCB traces. Measurement force (power) and sense (measure) lines should be kept independent of each other from the edge connector to the package terminals. Vias between "signal traces" and the buried planes are allowed for power and ground connections only and must be outside of the fan-out traces.

1s and 2s2p PCB: To route a signal from the interior of a large array to the edge connector, it may be necessary to use a via adjacent to the signal ball and a trace on the backside of the PWB. This is acceptable if the total width of traces, both topside and backside, connected to balls of the same row, does not exceed the total specified in 5.3. The via, via pad and isolation clearance shall be sized in accordance with 5.5. The via must be isolated from any internal copper planes. The trace shall be routed directly beneath the topside traces for the balls of the same row until outside the fan-out region.

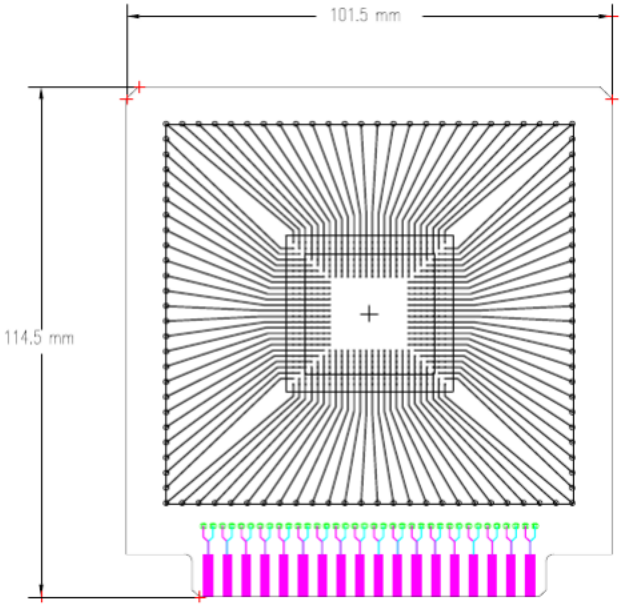


Figure 6 — Nesting of 256 and 352 PBGA packages.

5 Trace design (cont'd)

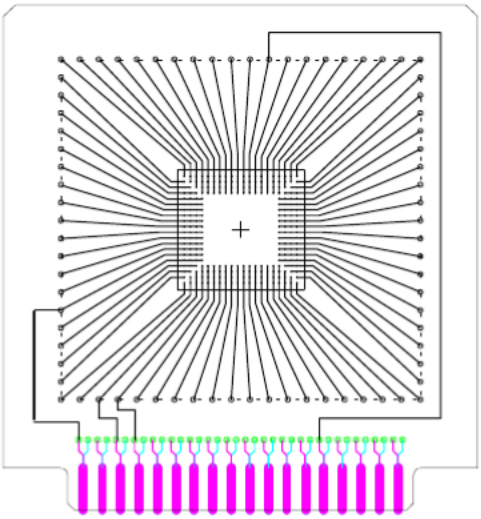


Figure 7 — Routing outside fan-out layer allowed in low conductivity PCB. High conductivity PCB allows any routing needed on bottom trace layer while the top routing must remain outside the fan-out region.

5.7 Buried layer layout (2s2p PCB only)

The power and ground planes embedded in the board shall be of 35 ∝m (1 oz.) copper +0/-20%. They are to be continuous except for via isolation clearance patterns. The power and ground planes shall terminate 1.0 mm from the edges of the PCB, giving overall plane dimensions as listed in table 3. The power and ground planes must not be present in the 9.5 mm edge connector pattern location shown in figure 2.

Table 3 — PCB buried plane sizes

PCB Size (+/- 0.25 mm)	Buried Plane Size
101.5 mm x 114.5 mm	99.5 mm x 99.5 mm
127.0 mm x 139.5 mm	125.0 mm x 125.0 mm
152.5 mm x 165.0 mm	150.5 mm x 150.5 mm

5.8 PCB metalization characteristics for 1s and 2s2p PCBs

For packages with ball pitch > 0.5 mm, the top and bottom trace metalization on the PCB shall be 70 ∝m (2 oz) +/- 20% finished thickness after final processing. For packages with ball pitch ″ 0.5 mm, the top and bottom trace metalization on the PCB shall be 50 ∝m (1.5 oz) +/- 20% finished thickness after final processing. This is achieved by starting with a 1 oz copper material and plating up to the target thickness during PCB through hole plating process. This process specification should be printed on all drawings to ensure proper processing. The thickness of the copper traces shall be verified to +/- 20% after PCB fabrication because thickness variations greater than this can have an excessive influence on the performance of the PCB.

5 Trace design (cont'd)

5.9 Solder masks for 1s and 2s2p PCBs

Solder masking is not optional and must follow the constraints described for the ball lands in 5.3.

5.10 Plated through-hole vias for 1s and 2s2p PCBs

The plated through-hole vias at the border of the trace fan-out area and beyond shall have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter. A block out area or isolation clearance of diameter no greater than 0.70 mm larger than the drill hole diameter shall exist in the buried solid planes around each plated through-hole via. Other than this isolation clearance area, the buried planes are to be unbroken. Some buried plane copper must exist between via isolation clearance regions; the clearance regions are not to merge into one another.

6 Hand wiring

Connection to edge connector: Connection from the through-holes to the edge connector shall be made with 22AWG copper wire or smaller if the connections are not designed as part of the trace pattern. When the board is intended for use in forced air measurement environments, interconnect wiring to the edge connector shall be on the trailing edge of the board with respect to air flow direction and back side of the board with respect to the component placement. Interconnect wiring shall be outside the fan-out area. Figure 8 shows a suggestion for wiring from the leading edge of the test board to the trailing edge before being routed to the edge connector. Connection from the edge connector to the fan-out perimeter and from the fan-out perimeter to the power dissipation structures must be made in a four-point method for force (power) and sense (measure) purposes. Wire diameters for heating force currents may need to be larger to accommodate high power tests and may require more than one edge connector pin. Use table 4 as a guide to determine the required wire diameter [5,6].

Table 4 — Wire size current limits

AWG Wire Size	UL Current Capacity, (80 ºC), Amperes	MIL-W-5088B Amperes
30	0.4	N/A
28	0.6	N/A
26	1.0	N/A
24	1.6	N/A
22	2.5	5.0
20	4.0	8.3
18	6.0	15.4
16	10.0	19.4
14	16.0	31.2
12	26.0	40.0

6 Hand wiring (cont'd)

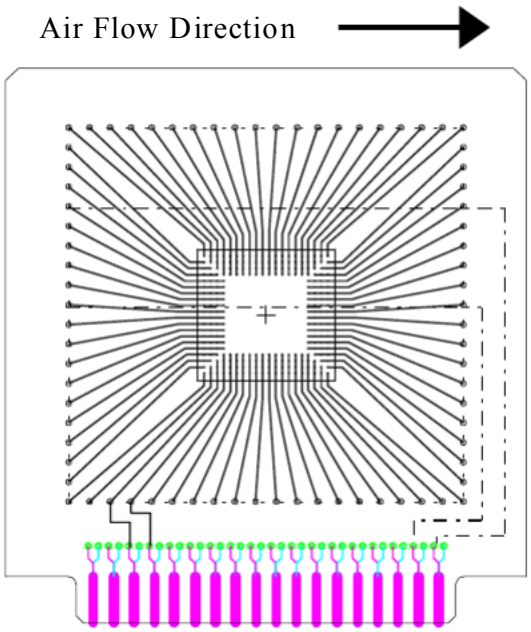


Figure 8 — Dashed lines show hand wiring across back of test board to avoid interupting air flow on leading edge of board for air flow measurement environments.

7 Data presentation

Table 5 lists parameters specified by this document. The "user" column allows the user to input actual measured values from the test boards.

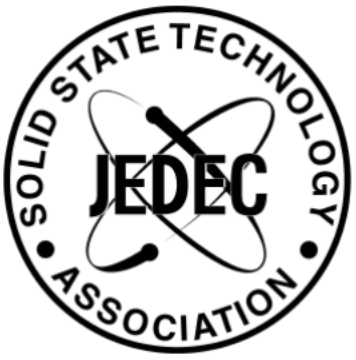
Table 5 — Specified parameters and values used

	Dimension	Specification	User
1	Board Finish Thickness	1.60 mm +/- 10%	
2	Board Dimension (+/- 0.25 mm)	❑ 101.5 mm x 114.50 mm [PKG ″ 40 mm] ❑ 127.0 mm x 139.50 mm [40 < PKG ″ 65 mm] ❑ 152.5 mm x 165.0 mm [65 < PKG ″ 90 mm]	
3	Board Material	FR-4	
4	Dielectric Layer Thickness	0.25 mm ″ thickness ″ 0.5 mm	
5	Fan-out Trace Length from PKG body (minimum)	25 mm	
6	Fan-out Trace Position	❑ centered in 101.5 mm x 101.5 mm section [PKG ″ 40 mm] ❑ centered in 127 mm x 127 mm section [40 < PKG ″ 65 mm] ❑ centered in 152.5 x 152.5 mm section [65 < PKG ″ 90 mm]	
7	Trace Copper Thickness	70 ∝m +/-20% for > 0.5 mm ball pitch, 50 ∝m +/-20% for ″ 0.5 mm ball pitch	
8	Finished Trace Width	36% to 44% of ball pitch for pitches > 0.5 mm 45% to 55% of ball pitch for pitches ″ 0.5 mm	
9	Trace Coverage Area (total)		
10	Nested?	yes/no: package body sizes nested	
11	Backside Interconnect?	yes/no	
13	Multilayer (buried pwr/gnd)	yes/no	
14	Power/Ground Thickness	35 ∝m (1oz) copper +0/-20%	
15	Power/Ground space to PCB edge	1 mm	
16	Power/Ground connected to fan-out vias?	yes/no: number of connections	
17	Number of ball rows connected		
18	Number of backside traces		
19	Number of thermal ball pads		
20	Solder Mask (required)	type	
21	Number of Thermal Vias		
22	Thermal Vias in Nested Pattern?	yes/no	
23	Thermal Via Outer Diameter	per table 2	
24	Thermal Via Isolation Clearance Diameter	0.20 mm > via diameter minimum, continuous buried plane through isolation pattern	

7 Data presentation (cont'd)

Table 5 — Specified parameters and values used (cont'd)

	Dimension	Specification	User
26	Number of Thermal Vias to Top Plane	(2s2p PCB only)	
27	Number of Thermal Vias to Bottom Plane	(2s2p PCB only)	
28	Fan-out Trace Via Spacing	≥ 2.54 mm	
29	Fan-out Trace Via Land	1.25 mm	
30	Fan-out Trace Via Drill Hole	0.85 mm	
31	Fan-out Trace Via Isolation Clearance	″ 0.70 mm oversize of via hole; buried plane continuity assured through via regions	
32	Wire Gauge (Sense)	″ 22AWG	
33	Wire Gauge (Heater Force)	See Table 4	
34	Heater sense lines merged with force lines?	❑ on die ❑ in package ❑ on PWB	
35	TSE sense lines merged with force lines?	❑ on die ❑ in package ❑ on PWB	
36	Drawings Available?	Yes/no	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