JEDEC STANDARD

Integrated Circuit Thermal Test Method Environmental Conditions — Junction-to-Board

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JEDEC Solid State Technology Association

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INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS – JUNCTION-TO-BOARD

CONTENTS

INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS – JUNCTION-TO-BOARD

(From JEDEC Board Ballot JCB-99-09, formulated under the cognizance of the JC15.1 Committee on Thermal Characterization.)

1 Scope

This standard specifies the environmental conditions necessary for determining the junction-to-board thermal resistance, $R_{\theta JB}$, and defines this term. The $R_{\theta JB}$ thermal resistance is a figure of merit for comparing the thermal performance of surface mount packages mounted on a standard board. This specification should be used in conjunction with the overview document JESD51, "Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)" [1] and the electrical test procedures described in EIA/JESD51-1, "Integrated Circuit Thermal Measurement Method (Single Semiconductor Device)" [2]. The environmental conditions described in this document are specifically designed for testing of integrated circuit devices that are mounted on standard test boards with two internal copper planes [3]. This standard is not applicable to packages that have asymmetric heat flow paths to the printed circuit board caused by such thermal enhancements as fused leads (leads connected to the die pad) or power style packages with the exposed heat slug on one side of the package.

2 Normative references

The following standards contain provisions that, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

[1] JESD51, “Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)”

[2] JESD51-1, “Integrated Circuit Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device)”

[3] JESD51-7, “High Effective Thermal Conductivity Test for Leaded Surface Mount Packages”

[4] JESD51-6, “Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)”

3 Definitions, symbols, and abbreviations

For the purposes of this standard, the following definitions apply:

shadow: maximum overall dimensions on the board that would be occupied by the package. For the BGA package, the shadow is the substrate size. For a QFP package, the shadow is the lead tip to tip size.

$R_{\theta JB}$: Junction-to-board thermal resistance as defined in this specification. θ_{JB} is an alternate symbol. When Greek letters are not available, the symbols are typed as RthJB or Theta-JB.

Ψ_{JB}: Junction-to-board thermal characterization parameter measured using the method defined in Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air) [5]. When Greek letters are not available, the symbol is typed as Psi-JB.

TSP: Temperature-sensitive parameter

Refer to the document JESD51, JESD51-1, and JESD51-2 for a general list of terminology.

4 Specification of environmental conditions

4.1 Thermal test board

The printed circuit board used to mount the devices shall be specified in JESD51-7 "High Effective Thermal Conductivity Test for Leaded Surface Mount Packages" [3]. This specification can be extended to testing other surface mount integrated circuit packages with the appropriate test board specification with two internal planes.

4.2 Ring style cold plate

The ring style cold plate is a fluid cooled cold plate that clamps both sides of the test board such that the heat flows from the package radially in the plane of the test board.

4.2.1 Material

The cold plate is machined from copper or copper alloy (conductivity greater than 300 W/m•K such as C14500 or C14700) and then nickel plated. The ring style cold plate is illustrated in figures 1 and 2. There is a square hole in the cold plate to accommodate the package.

4.2 Ring style cold plate (cont'd)

4.2.2 Clamp location

The cold plate is clamped onto the solder mask covered traces on the board at a minimum of 5 mm from the package (the shadow of the package). The package shall be centered +/- 10% of the distance from the package shadow to the clamp. The cold plate clamp area must be a minimum of 4 mm wide. The test board design must have the vias for hand soldered jumper wires close enough to the edge of the board that the vias will not interfere with clamping of the cold plate. Clamping force should be evenly applied and be sufficient that the board will not move with respect to the ring if a 200 gram force is applied to the board. The measurement results are not sensitive to clamping force. Thermal grease does not have to be used.

4.2.3 Example designs

Examples of the ring cold plate design are included as figures A1 and A2 in annex A.

4.3 Insulation requirements

The package opening in the top and bottom of the cold plate are insulated. The insulation material with a conductivity less than 0.1 W/m•K is faced with a low emissivity aluminized plastic film. There should be a 1 to 5 mm air gap between the package and the insulation and between the bottom of the test board and the insulation on the bottom of the fixture. If solder mask over the traces on the board do not provide sufficient electrical insulation, tape not exceeding 0.075 mm in thickness may be used to electrically insulate the board traces such that the package can be tested.

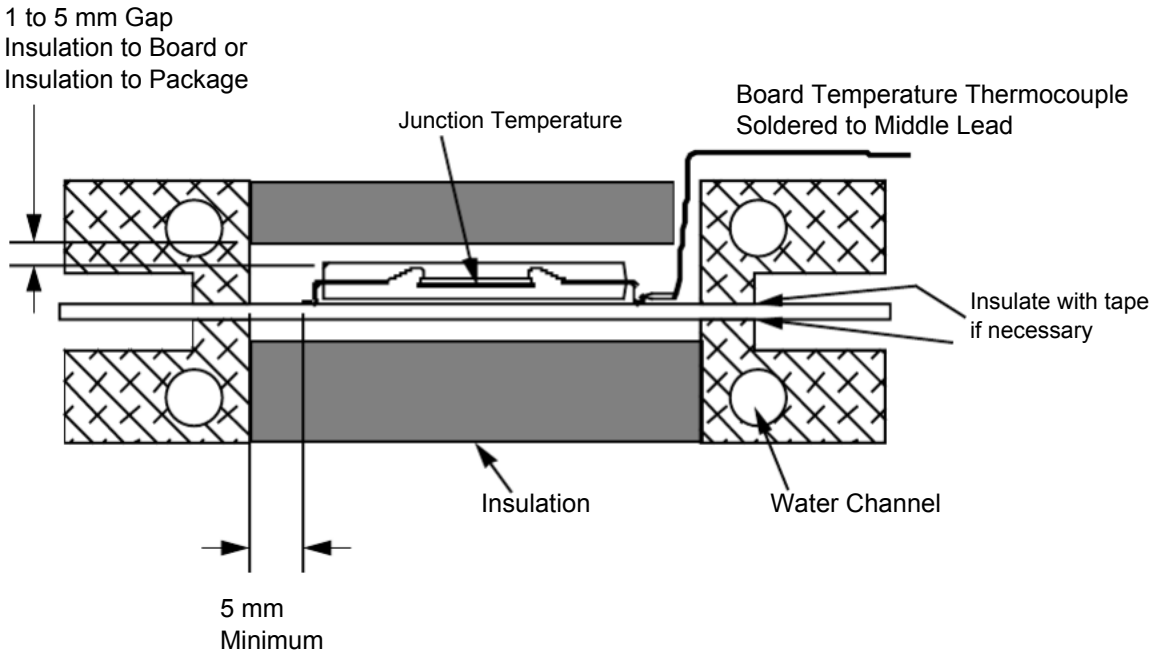

Figure 1 — Illustration of the ring style cold plate $R_{\theta JB}$ test fixture in cross section

4.3 Insulation requirements (cont'd)

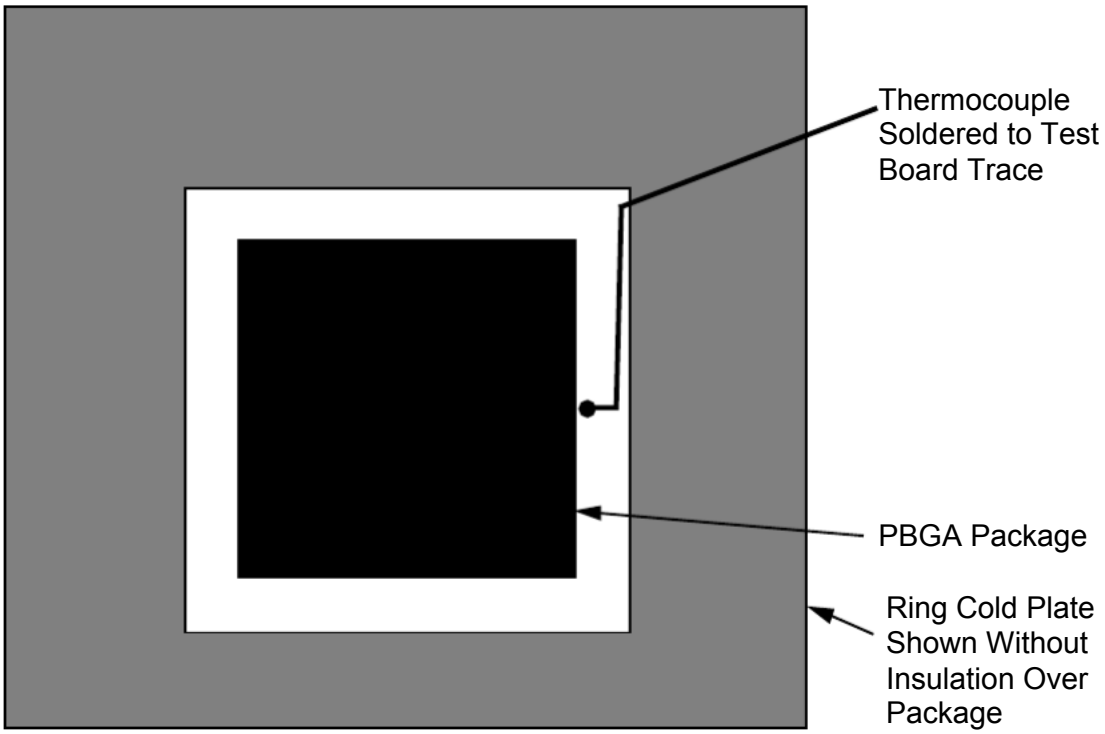

Figure 2 — Top View with the insulation removed
(To simplify the illustration, the traces on the test board are not shown. The thermocouple is attached to a board trace at the edge of the package in the location shown.)

4.4 Fluid temperature

The incoming cooling fluid should be controlled at the ambient room temperature in a range of +2 °C to -5 °C such that it does not change temperature more than 0.2 °C during the test. In addition, the block temperature where it contacts the board shall be uniform within 0.4 °C. Variations in block temperature are more likely a problem when using low specific heat dielectric fluids.

4.5 Board temperature measurement

The board temperature for this measurement shall be determined by a 40 gauge thermocouple which is soldered in place. Since type T thermocouples are easily soldered, type T is preferred. Type J or K may be also be used. Contact to the board trace or package lead foot should be verified by electrical conductivity. To reduce temperature gradients in the wire approaching the thermocouple junction, a small amount of thermally conductive epoxy is placed over the thermocouple junction and about one mm of wire extending from the thermocouple junction. The epoxy dot shall be no larger than 3 mm in diameter. The thermocouple meter must electrically float the thermocouple to avoid electrical interactions with any voltages applied to the package during test.

4.5 Board temperature measurement (cont'd)

For a leaded package, the thermocouple is attached to the foot of a package lead halfway along the side of the package. For a rectangular package, the lead is on one of the longer sides. The thermocouple is attached to the lead foot where the lead is joined to the test board. For an area array surface mount package, the thermocouple is attached to a test board trace halfway along one side of the package. The solder mask should be removed to allow attaching the thermocouple directly to the trace. The trace should be a trace to which the package is soldered. The thermocouple junction must be within 1 mm of the package body.

Although the measurement is not applicable to packages with asymmetric heat flow paths to the printed circuit board, caused by such thermal enhancements as fused leads (leads connected to the die pad) or power style packages with exposed heat slug on one side of the package, there are cases where the fused leads cause a relative minor asymmetry in the heat flow. For those cases, if that center lead is stamped or etched from the same piece of material as the die pad in a "thermal lead" or "fused lead" configuration, the lead adjacent to the "fused lead" is used for the measurement.

5 Measured and calculated parameters

5.1 Junction-to-board thermal resistance

The junction-to-board thermal resistance is determined from equation (1):

$$R_{\theta JB} = (T_J - T_B)/P_H \quad (1)$$

where

$R_{\theta JB}$ = thermal resistance (°C/W) from junction-to-board as described by this specification
T_J = junction temperature (°C) when the device has achieved a steady-state after application of P_H
T_B = board temperature (°C) at steady state
P_H = power dissipation (W) which produced the change in junction temperature

5.2 Temperature-sensitive parameter

As described in the reference [2], a temperature-sensitive parameter (TSP) is used to sense the change in temperature of the junction operating area due to the application of electrical power to the device. In equation terms,

$$\varnothing T_J = (\varnothing TSP \times K_{factor}) \quad (2)$$

where

$\varnothing TSP$ = change in the TSP caused by the application of P_H
K_{factor} = is the quotient of the junction temperature change to the temperature sensitive parameter change in the linear region of the temperature-sensitive parameter temperature relationship, typically specified in units of °C/mV; usually applicable to semiconductor devices using a forward biased temperature sensitive parameter.

5.3 Determination using K_{factor}

The junction-to-board thermal resistance can then be determined by equation (3):

$$R_{\theta JB} = (T_{B0} + [\varnothing TSP \times K_{factor}] - T_{BSS})/P_H \quad (3)$$

where

T_{B0} = Initial board temperature before heating power is applied
T_{BSS} = Final board temperature when steady state has been reached.

5.4 Calibration equation

A calibration equation may also be used to determine the junction temperature as specified in reference [2].

6 Test Procedure

6.1 TSP calibration

Prior to making actual thermal measurements, the temperature-sensitive parameter shall be empirically calibrated using the procedure in section 3.3 of the reference [2].

6.2 Thermal equilibrium

Place the package and test board in the ring cold plate. Prior to recording the initial conditions of the thermal test, verify that the device has reached a state of equilibrium with the ambient temperature. To verify that stabilization has occurred, wait an initial 5 minutes minimum, then record the TSP, wait an additional 5 minutes and record a second TSP. If $\varnothing T_J$ as determined by the TSP measurement is less than or equal to 0.2 °C, then equilibrium has been achieved. If equilibrium has not occurred, then continue for additional 5 minute intervals.

6.3 Initial readings

After equilibrium has been reached, record the values for the TSP and the initial board temperature T_{B0}.

6.4 Apply power

The power levels shall be chosen such that the junction temperature rise during testing is between 15 °C and 30 °C. Apply the heating voltage (V_H) and the heating current (I_H) to the device.

6.5 Steady state

For a test measurement to be completed, verification that thermal steady state has been reached shall be done before the final readings can be taken. Steady-state shall be determined as required in section 3.6 of reference [2].

6.6 Steady state measurements

After a steady-state has been reached, record the values for the TSP, the heater voltage (V_H), the heater current (I_H), the time required to reach steady state (t_{Hss}), and the final board temperature at the end of the test (T_{Bss}).

7 Usage

7.1 Thermal simulation models

The junction-to-board thermal resistance, $R_{\theta JB}$, will find use as an indicator of thermal performance for incorporation into board level thermal simulation models. How the information is used in a board level simulation and the resulting accuracy will depend on the simulation software. Since $R_{\theta JB}$ is primarily a figure of merit, the resulting accuracy of the board level simulations will be less than could be obtained with a more detailed model.

7.2 Simulation validation

Another use of $R_{\theta JB}$ will be the validation of package simulation models by providing defined boundary conditions for simulation. Since the thermal test board can contribute up to 50% of the thermal resistance measured in this test, it is required that the test board be accurately modeled. Actual physical measurements of the test board are needed for accurate models. The junction-to-board determined by this specification must not be confused with similar measurements obtained with the "double cold plate" apparatus.

7.3 Ψ_{JB} junction-to-board thermal characterization parameter

Junction-to-board thermal resistance, $R_{\theta JB}$, must not be confused with a junction-to-board thermal characterization parameter, Ψ_{JB}, determined using the methods specified in "Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)". Frequently, the junction-to-board thermal resistance will be larger than junction-to-board thermal characterization parameter.

8 Test conditions to be reported

The values listed in table 1, which are needed to describe this test and the results, must be reported when publishing.

Table 1 — Thermal measurement test conditions and data parameters

Measurement Area	Condition Parameters	Data Parameters and Results
Device Identification		Device Identification Date
Environmental	Cold Plate Drawing number Test Board Specification (and drawing number) Thermocouple Type and gauge Thermocouple attachment location	
Measurements	T_{B0} (°C) T_{BSS} (°C) V_H (V) I_H (mA) t_{Hss} (s) I_m (mA) K_{factor} (°C/mV)	V_f (V) $\varnothing T_J$ (°C) P_H (W) $R_{\theta JB}$ (°C/W)

Annex A – Ring cold plate design example

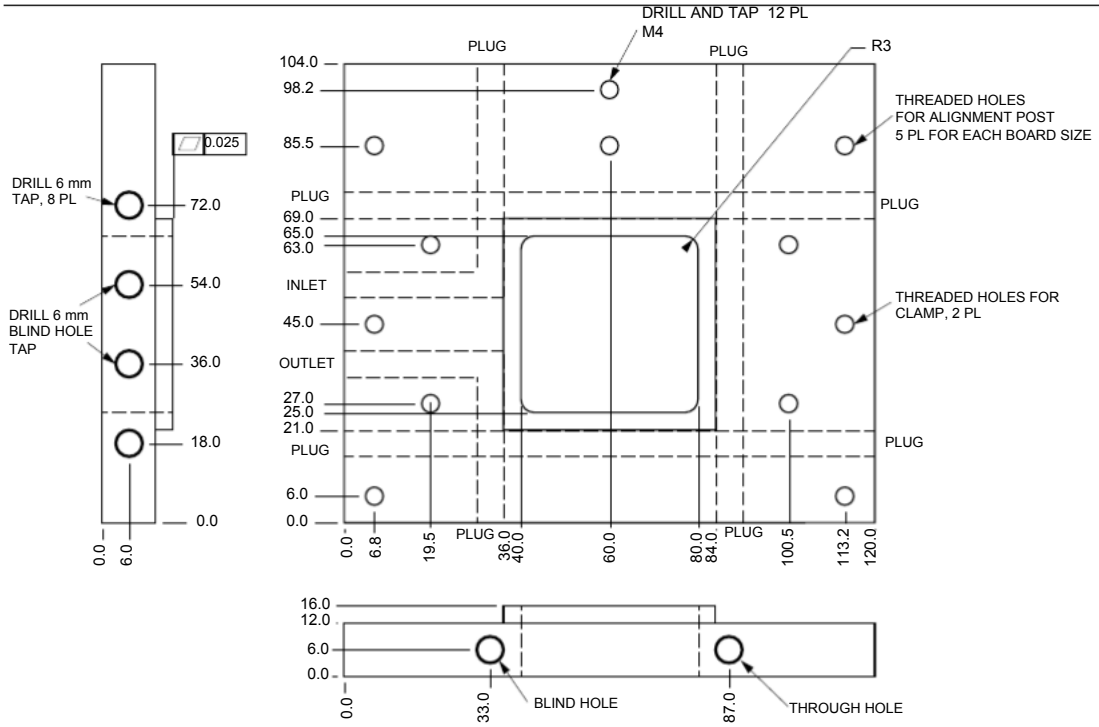

Figure A1a - Drawing of bottom piece of ring cold plate fixture designed for packages with footprint less than 30 mm in longest dimension. Fabricated from copper and then nickel plated. All dimensions are basic. If 8-32 screws are used instead of M4 to center the test board, threaded holes should be moved 0.1 mm further from the center line of the fixture. Only the externally visible drilled holes are shown in side views.

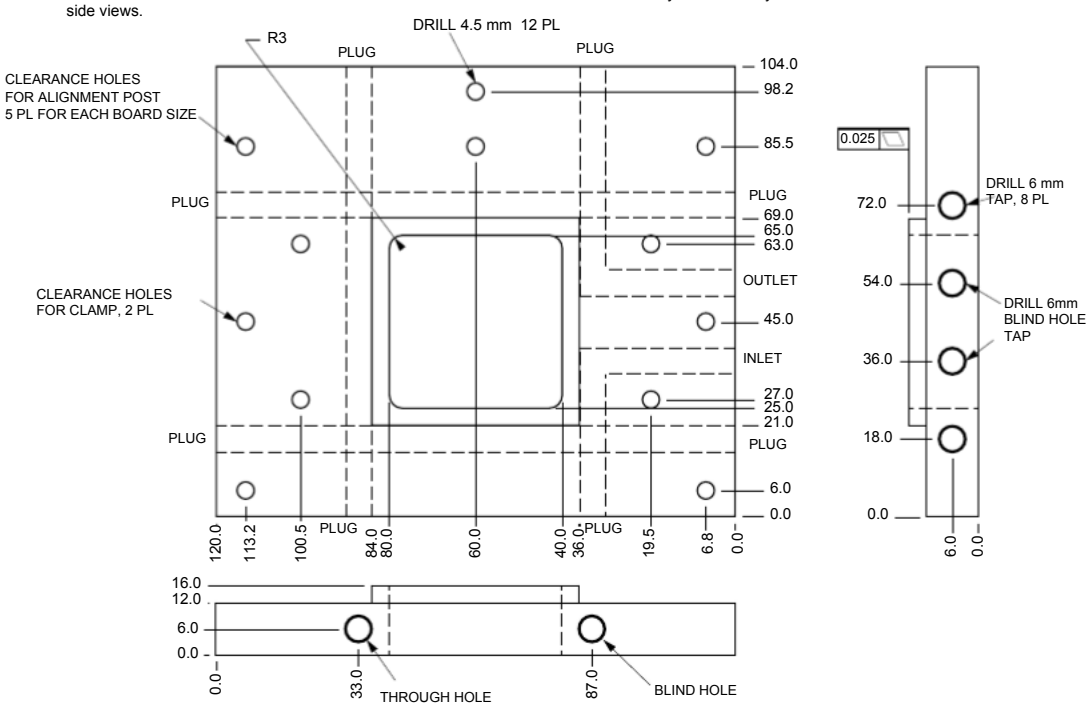

Figure A1b - Drawing of top piece of the ring cold plate fixture designed for packages with footprint less than 30 mm in longest dimension. Top piece is shown upside down for easy of documenting dimensions. Refer to figure 1 to illustrate assembly. Fabricated from copper and then nickel plated. All dimensions are basic. Only externally visible drilled holes are shown in side views.

Annex A – Ring cold plate design example

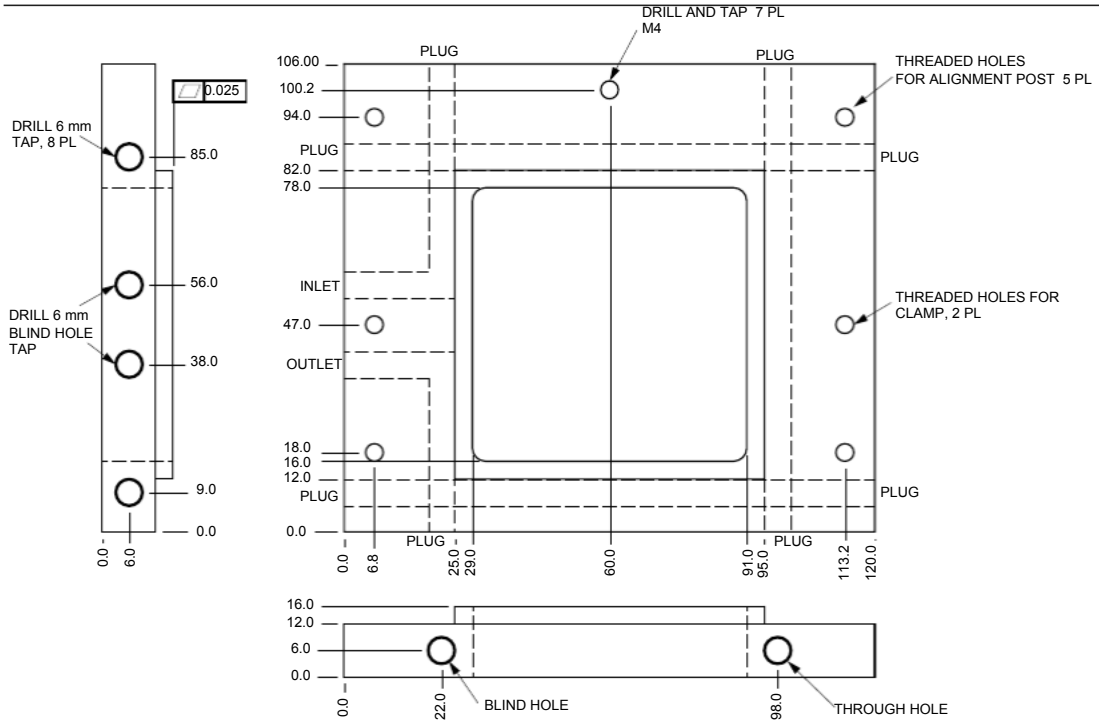

Figure A2a - Drawing of bottom piece of ring cold plate fixture designed for packages on 101.6 mm test board. Fabricated from copper and then nickel plated. All dimensions are basic. Only the externally visible drilled holes are shown in the side views.

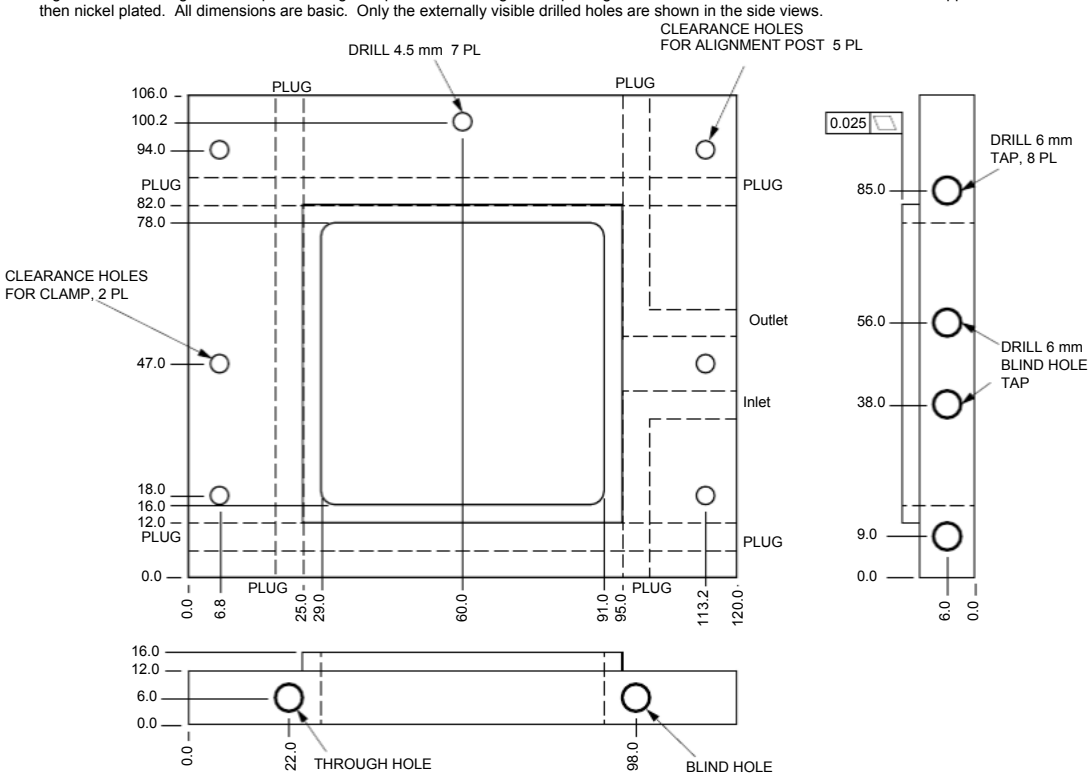

Figure A2b - Drawing of top piece of ring cold plate fixture designed for packages on 101.6 mm test board. Fabricated from copper and then nickel plated. All dimensions are basic. Only externally visible drilled holes are shown in the side views.