JEDEC STANDARD

Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements

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TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENTS

CONTENTS

Foreword

The measurement of the junction-to-ambient ($R_{\theta JA}$) thermal characteristics of an integrated circuit (IC) has historically been carried out using a number of test fixturing methods. The most prominent method is the soldering of the packaged devices to a printed circuit board (PCB). The characteristics of the test PCBs can have a dramatic (>60%) impact on the measured $R_{\theta JA}$. Due to this wide variability, it is desirable to have an industry-wide standard for the design of PCB test boards to minimize discrepancies in measured values between companies.

To obtain consistent measurements of $R_{\theta JA}$ from one company to the next, the test PCB geometry and trace layout must be completely specified for each package geometry tested. Such a complete specification would limit the flexibility of user companies who would like to design test boards for their individual needs. Thus, one characteristic of a test board specification is to allow some variability of PCB test board design while minimizing measurement variability.

This specification is intended for use with the thermal measurements and modeling specifications grouped under JEDEC EIA/JESD 51, [1]. Specifically, the electrical test procedures described in JEDEC EIA/JESD 51-1, “Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device),” [2], and 51-2, “Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air), [3], and 51-6, “Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air), [4].

TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENTS

(From JEDEC Board Ballot JCB-00-59, formulated under the cognizance of the JC-15.1 Subcommittee on Thermal Characterization.)

1 Scope

This specification covers through-hole area array leaded packages intended to be mounted on a PCB. It does not cover area array packages that require sockets.

2 Normative references

[1] JESD 51, *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).*

[2] JESD 51-1, *Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device).*

[3] JESD 51-2, *Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air).*

[4] JESD 51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air).*

[5] *Electronics Engineer's Handbook*, 3rd Edition, Edited by D.G. Fink and D. Christiansen, McGraw-Hill Book Co., NY, 1989, p 6.16

[6] *MIL-W-5088L, Amdt. 1*, Wiring, Aerospace Vehicle

[7] IPC-2222, *Sectional Design Standard for Rigid Organic Printed Boards*

[8] IPC-2221, *Generic Standard on Printed Board Design*

3 Stock material

The PCB test board shall be made of FR-4 material. The finish size shall be 1.60 mm +/- 10% thick. For high ambient or board temperature applications (> 125 ºC), use of other test board material is acceptable as long as the thermal conductivity of the material is reported and measurement correlations have been established between the substitute material and FR-4.

Trace thickness is achieved by starting with standard copper stock and then plating to final thickness. A convention in PCB fabrication is to refer to copper thickness using the terminology ounces of copper per square foot of board. An ounce of copper per square foot translates to a copper thickness of 35 ∝m.

The 1s test board has only a top trace layer in the component mounting and trace fan-out region (see figure 1a). The copper trace thickness shall be 70 ∝m (2 oz) +/- 20%. A bottom trace layer may be used for solder lands at the end of the fan-out traces and edge connection points. Connection to the edge connector outside the package fan-out region can be made with either the top or bottom signal traces. The 2s2p version of this test board is formed by embedding two 35 ∝m (1 oz) +0/-20% copper planes in the PCB (as shown in figure 1b), while maintaining the finished thickness at 1.60 mm.

Figure 1a — Cross section of 1s PCB showing trace and dielectric thicknesses in package placement and trace fan-out regions

Figure 1b — Cross section of 2s2p PCB showing trace and dielectric thicknesses

4 Board outline

The board shall be 101.5 mm x 114.5 mm +/- 0.25 mm in size for packages less than or equal to 40 mm on a side (see figure 2). A typical edge connector is depicted in figure 2. The edge connector can be pin-out and pitch modified for specific needs. Modification of the width dimension of the edge connector is allowed. Multiple rows of vias along the edge connector are allowed.

For various package sizes, refer to table 1 for the appropriate PCB size.

Table 1 — PCB sizes for packages

Package Length	PCB Size (+/- 0.25 mm)
Pkg. Length ″ 40 mm	101.5 mm x 114.5 mm (4.0 in x 4.5 in)
40 mm < Pkg. Length ″ 65 mm	127.0 mm x 139.5 mm (5.0 in x 5.5 in)
65 mm < Pkg. Length ″ 90 mm	152.5 mm x 165.0 mm (6.0 in x 6.5 in)

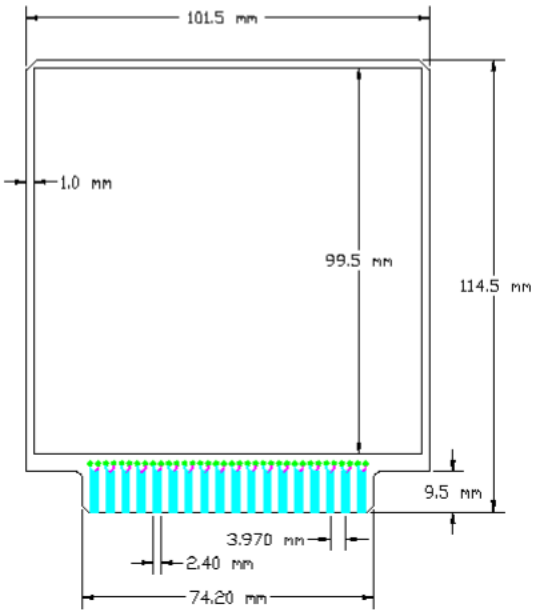

Figure 2 — Example test board outer dimensions and edge connector design

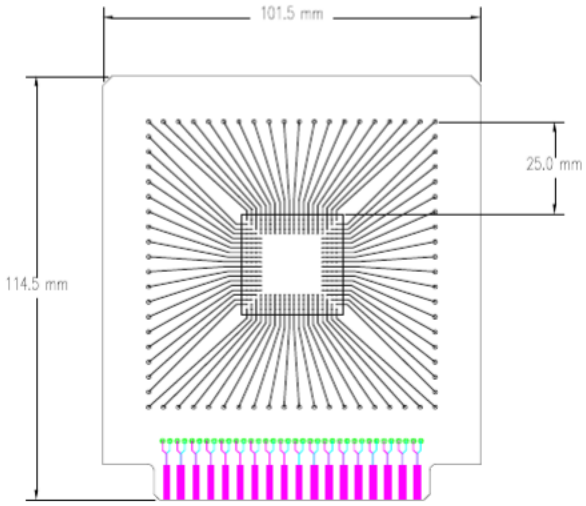

Figure 3 — Traces to outer pin row flared to perimeter 25 mm from package body.

5 Trace design

5.1 Top trace layer layout (both 1s and 2s2p PCBs)

Traces should be laid out such that the test device will be centered relative to a 101.5 mm x 101.5 mm section towards the top of the board (away from the edge connector) for the smallest board. For larger board sizes, locate the package at the top of the board in the center of a square whose length is the width dimension of the board. The traces connecting to the package must extend at least 25 mm out from the edge of the device body. Trace lengths longer than this amount are allowed. Traces must be routed in a radial fashion (flared) to meet the edges of a rectangle such that the terminal via locations are equally spaced over 90% of the perimeter of the sides of this rectangle. Traces must be flared out to the 25 mm perimeter adjacent to the side of the package they are on. Corner-most lands flare to the perimeter clockwise of the corner (see figure 3). Staggering of trace terminal soldering positions inward from the trace termination rectangle is allowed to 2.5 mm off the perimeter of the square.

Traces must short all pin rows on a given side of a package together as shown in figure 4. If the package interposer is designed so that two connections needed for the thermal test would be shorted when the pin rows are shorted together, the trace may be cut to eliminate the short (see figure 4a). No more than 10% of the total number of traces should be cut. Routing two traces per pin position is allowed (as shown in figure 4d) as long as the total trace width per pin position in the fan-out region is as specified in 5.2. The routing of figure 4d may require the use of traces that are narrower than specified in 5.2 in the pin array area. This is allowed as long as the trace portion outside of the package body is in agreement with the width specified by 5.2. A trace design that nests packages with equal pin pitches on the same PCB is allowed as long as the above conditions are met (see figure 5).

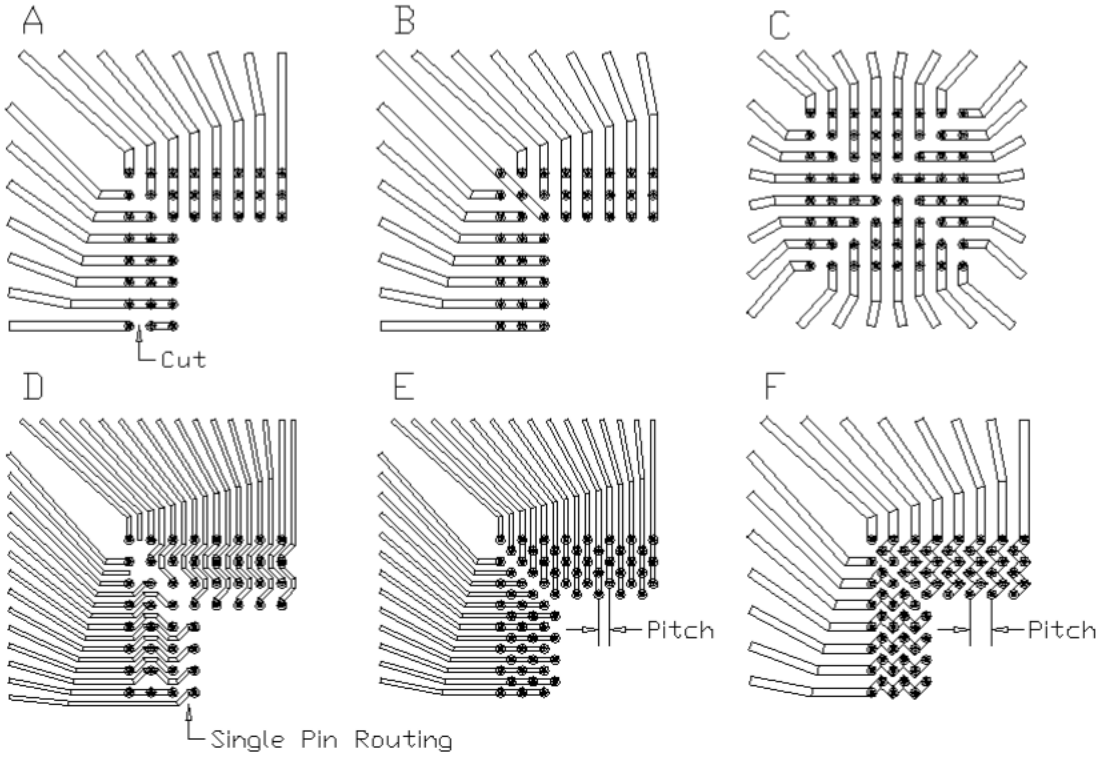

Figure 4 — Examples of trace routing

5 Trace design (cont'd)

5.2 Trace widths for 1s and 2s2p PCBs

Finished trace widths shall be from 36% to 44% of the nominal pin pitch. For multiple trace per pin position designs (e.g., figure 4d), the combined total trace width shall not be greater than 40% of the pin pitch and each trace shall be of equal width. Splitting of traces in two parts, e.g. in order to keep force (power) and sense (measure) lines independent, is allows as long as their summed widths meets the above specified total trace width. For staggered arrays, the trace width may be based on the staggered pitch (see figure 4e) or on the inline pitch (see figure 4f). Achieving the finish size may require some oversize in design to compensate for overetching of the copper traces during processing. Traces should terminate in plated through-holes for soldering interconnect purposes. See 5.3 for a description of the plated through-hole vias.

5.3 Plated through-hole vias

Vias for package mounting: The finished (plated) diameter for all plated through-holes used for package mounting shall be no less than the maximum pin diameter plus 0.15 mm and no more than the minimum pin diameter plus 0.60 mm [7]. For rectangular pins, the diameter shall be calculated as equal to the diagonal of the rectangular cross-section of the lead. The via pad diameter is specified in reference [8]. The nominal via pad diameter tolerance shall be +0.10/-0 mm.

For example, for a PGA (e.g., JEDEC MO-066) with the following dimensions:

Min. lead diameter: 0.25 mm
Max. lead diameter: 0.50 mm

The plated through-hole vias are as follows:

Min. finished hole diameter: 0.50 + 0.15 = 0.65 mm [7]
Max. finished hole diameter: 0.25 + 0.60 = 0.85 mm [7]
Via pad diameter: 0.85 + 0.20 + 0.10 = 1.15 +0.10/-0 mm [8]

The drill hole diameter shall be such as to yield the finished hole diameters specified above. An isolation clearance region with a diameter at least 0.2 mm larger than the drill hole diameter shall exist in the buried solid planes around each plated through-hole via. Other than this isolation clearance area, the buried planes are to be unbroken. Some buried plane copper must exist between via isolation clearance regions; the clearance regions are not to merge into one another. Except for any thermal pins (see 5.4), all package mounting vias shall be isolated from any buried solid planes.

Trace fan-out vias: The plated through-hole vias at the border of the trace fan-out area and beyond shall have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter. A block out area or isolation clearance of diameter no greater than 0.70 mm larger than the drill hole diameter shall exist in the buried solid planes around each plated through-hole via. Other than this isolation clearance area, the buried planes are to be unbroken. Some buried plane copper must exist between via isolation clearance regions; the clearance regions are not to merge into one another.

5 Trace design (cont'd)

5.4 Trace layers and connection routing

1s PCB: The only pattern permitted within the flared perimeter (fan-out area) is the fan-out pattern and package footprint on the top trace layer. The bottom layer shall be used only for via termination and limited connection routing to the edge connector. Routing to the edge connector is allowed in either the top or bottom signal layers if the interconnection remains outside the flared perimeter of the through-holes (see figure 6). No traces, except as noted below, are allowed to run on the backside of the PCB within the flared perimeter of the through-holes. Power connection routing should be designed to minimize voltage drops and self-heating across the PCB traces. Measurement force (power) and sense (measure) lines should be kept independent of each other from the edge connector to the package terminals.

2s2p PCB: The top trace layer shall be used for fan-out and interconnection to the edge connector outside the fan-out perimeter. Any required interconnection routing to the edge connector can be made using the bottom trace layer and the top layer as long as the top layer interconnection remains outside the package fan-out region. Power connection routing should be designed to minimize voltage drops and self-heating across the PCB traces. Measurement force (power) and sense (measure) lines should be kept independent of each other from the edge connector to the package terminals. Vias between "signal traces" and the buried planes are allowed for power and ground connections only and must be at the end of the fan-out traces.

1s and 2s2p PCB: To route a signal from the interior of a large array to the edge connector, it may be necessary to use a trace on the backside of the PWB. This is acceptable if the total width of traces, both topside and backside, connected to pins of the same row, does not exceed the total specified in paragraph 5.3. The trace should be routed directly beneath the topside trace(s) for the balls of the same row until outside the fan-out region.

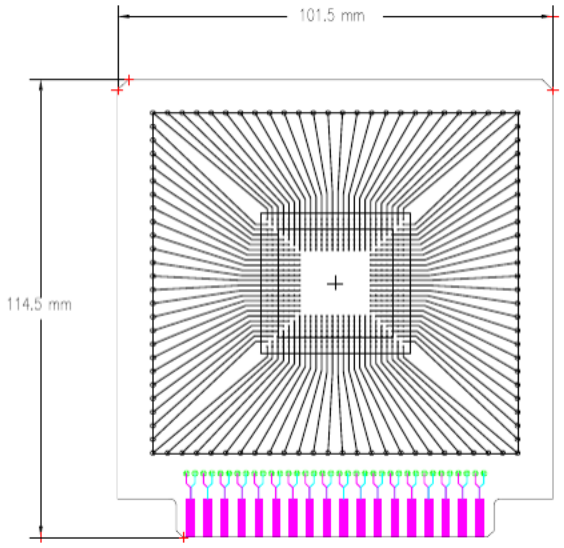

Figure 5 — Nesting of 256 and 352 PGA packages.

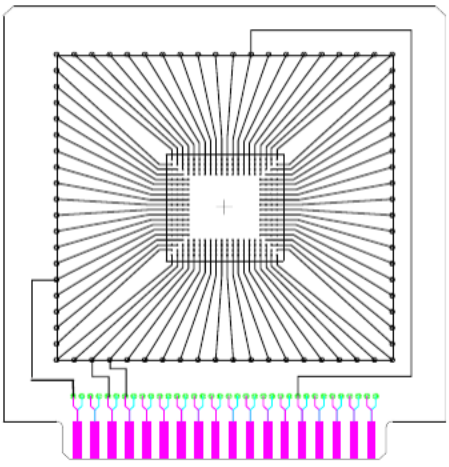

Figure 6 — Routing outside fan-out layer allowed in low conductivity PCB. High conductivity PCB allows any routing needed on bottom trace layer while the top routing must remain outside the fan-out region.

5 Trace design (cont'd)

5.5 Buried layer layout (2s2p PCB only)

The power and ground planes embedded in the board shall be of 35 ∝m (1 oz) copper +0/-20%. They are to be continuous except for via isolation clearance patterns. The power and ground planes shall terminate 1.0 mm from the edges of the PCB, giving overall plane dimensions as listed in table 2. The power and ground planes must not be present in the 9.5 mm edge connector pattern location shown in figure 2.

Table 2 — PCB buried plane sizes

PCB Size (+/- 0.25 mm)	Buried Plane Size
101.5 mm x 114.5 mm	99.5 mm x 99.5 mm
127.0 mm x 139.5 mm	125.0 mm x 125.0 mm
152.5 mm x 165.0 mm	150.5 mm x 150.5 mm

5.6 PCB metalization characteristics for 1s and 2s2p PCBs

Top and bottom trace metalization on the PCB shall be 70 ∝m (2 oz) finished thickness after final processing (0.070 mm). This is achieved by starting with a 1 oz copper material and plating to 2 oz during PCB through hole plating process. This process specification should be printed on all drawings to ensure proper processing. The thickness of the copper traces shall be verified to +/- 20% after PCB fabrication because thickness variations greater than this can have an excessive influence on the performance of the PCB.

5.7 Solder masks for 1s and 2s2p PCBs

Solder masking is required. Openings in the solder mask for the plated through holes shall be at least as large as the via pads without allowing them to merge into one another.

6 Hand wiring

Connection to edge connector: Connection from the through-holes to the edge connector shall be made with 22AWG copper wire or smaller if the connections are not designed as part of the trace pattern. When the board is intended for use in forced air measurement environments, interconnect wiring to the edge connector shall be on the trailing edge of the board with respect to air flow direction and back side of the board with respect to the component placement. Interconnect wiring shall be outside the fan-out area. Figure 7 shows a suggestion for wiring from the leading edge of the test board to the trailing edge before being routed to the edge connector. Connection from the edge connector to the fan-out perimeter and from the fan-out perimeter to the power dissipation structures must be made in a four-point method for force (power) and sense (measure) purposes. Wire diameters for heating force currents may need to be larger to accommodate high power tests and may require more than one edge connector pin. Use table 3 as a guide to determine the required wire diameter [5,6].

6 Hand wiring (cont'd)

Table 3 — Wire size current limits

AWG Wire Size	UL Current Capacity, (80 ºC), Amperes	MIL-W-5088L Amperes
30	0.4	N/A
28	0.6	N/A
26	1.0	N/A
24	1.6	N/A
22	2.5	5.0
20	4.0	8.3
18	6.0	15.4
16	10.0	19.4
14	16.0	31.2
12	26.0	40.0

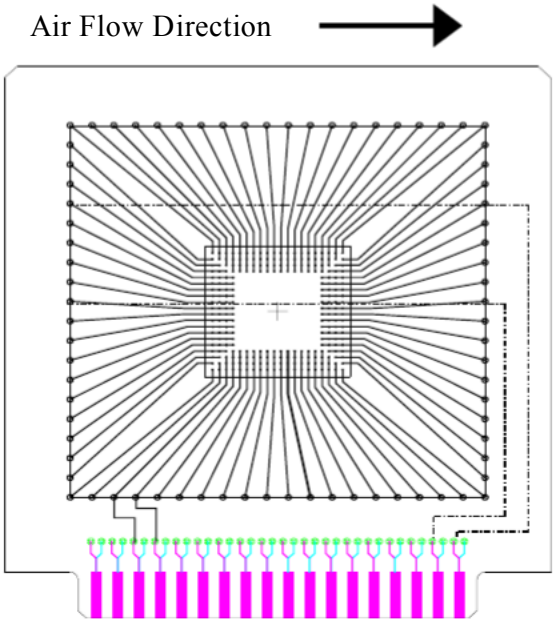

Figure 7 — Dashed lines show hand wiring across back of test board to avoid interrupting air flow on leading edge of board for air flow measurement environments.

7 Data Presentation

Table 4 lists parameters specified by this document. The "user" column allows the user to input actual measured values from the test boards.

Table 4 — Specified parameters and values used

	Dimension	Specification	User
1	Board Finish Thickness	1.60 mm +/- 10%	
2	Board Dimension (+/- 0.25 mm)	❑ 101.5 mm x 114.5 mm [PKG ″ 40 mm] ❑ 127.0 mm x 139.5 mm [40 < PKG ″ 65 mm] ❑ 152.5 mm x 165.0 mm [65 < PKG ″ 90 mm]	
3	Board Material	FR-4	
4	Dielectric Layer Thickness	0.25 mm ″ thickness ″ 0.5 mm	
5	Fan-out Trace Length from PKG body (min.)	25 mm	
6	Fan-out Trace Position	❑ centered in 101.5 mm x 101.5 mm section [PKG ″ 40 mm] ❑ centered in 127.0 mm x 127.0 mm section [40 < PKG ″ 65 mm] ❑ centered in 152.5 mm x 152.5 mm section [65 < PKG ″ 90 mm]	
7	Copper Trace Thickness	70 ∝m +/-20%	
8	Trace Width	From 36% to 44% of pin pitch	
9	Trace Coverage Area (total)		
10	Package Mount Via Finished Diameter	Minimum = maximum pin diameter + 0.15 mm Maximum = minimum pin diameter + 0.60 mm	
11	Package Mount Via Pad Diameter	Nominal as specified by reference [8].	
12	Package Mount Via Isolation Clearance	Drill diameter + 0.2 mm minimum	
13	Nested?	yes/no: package body sizes nested	
14	Backside Interconnect?	yes/no	
15	Number of backside traces		
16	Multilayer (buried pwr/gnd)	yes/no	
17	Power/Ground Thickness	35 ∝m (1oz) copper +0/-20 %	
18	Power/Ground space to PCB edge	1 mm	
19	Power/Ground connected to fan-out vias?	Yes/no: number of connections	
20	Number of pin rows connected		
21	Solder Mask (required)	Type	
22	Fan-out Trace Via Spacing	2.54 mm	
23	Fan-out Trace Via Land	1.25 mm	
24	Fan-out Trace Via Drill Hole	0.85 mm	
25	Fan-out Trace Via Isolation Clearance	″ 0.70 mm oversize of via hole; buried plane continuity assured through via regions	
26	Wire Gauge (Sense)	22AWG	
27	Wire Gauge (Heater Force)		
28	Heater sense lines merged with force lines?	❑ on die ❑ in package ❑ on PWB	
29	TSP sense lines merged with force lines?	❑ on die ❑ in package ❑ on PWB	
30	Number of Traces Cut		
31	Drawings Available?	Yes/no