# JEDEC STANDARD



# Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements

## JESD51-10

JULY 2000

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

## NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the EIA General Counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby an JEDEC standard or publication may be further processed and ultimately become an ANSI/EIA standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC Solid State Technology Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834, (703)907-7560/7559 or www.jedec.org

Published by
JEDEC Solid State Technology Association 2000
2500 Wilson Boulevard
Arlington, VA 22201-3834



**PRICE: Please refer to the current**
**Catalog of JEDEC Engineering Standards and Publications or call Global Engineering Documents, USA and Canada (1-800-854-7179), International (303-397-7956)**

Printed in the U.S.A.

PLEASE!

DON'T VIOLATE
THE
LAW!



JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

# TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE THERMAL MEASUREMENTS

## CONTENTS

## Foreword

The measurement of the junction-to-ambient ($R_{\theta JA}$) thermal characteristics of an integrated circuit (IC) has historically been carried out using a number of test fixturing methods. The most prominent method is the soldering of the packaged devices to a printed circuit board (PCB). The characteristics of the test PCBs can have a dramatic (>60%) impact on the measured $R_{\theta JA}$. Due to this wide variability, it is desirable to have an industry-wide standard for the design of PCB test boards to minimize discrepancies in measured values between companies.

To obtain consistent measurements of $R_{\theta JA}$ from one company to the next, the test PCB geometry and trace layout must be completely specified for each package geometry tested. Such a complete specification would limit the flexibility of user companies who would like to design test boards for their individual needs. Thus, one characteristic of a test board specification is to allow some variability of PCB test board design while minimizing measurement variability.

This specification is intended for use with the thermal measurements and modeling specifications grouped under the JEDEC EIA/JESD51 series, [1]. Specifically, the electrical test procedures described in JEDEC EIA/JESD51-1, "Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device)," [2], EIA/JESD51-2, "Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air), [3], and EIA/JESD51-6, "Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air), [4].


中国热管理网
www.reguanli.com

# TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE THERMAL MEASUREMENTS

(From JEDEC Board Ballot JCB-00-15, formulated under the cognizance of the JC-15.1 Subcommittee on Thermal Characterization.)

## 1 Scope

This specification covers through-hole mount perimeter leaded packages intended to be mounted on a PCB. It does not cover area array packages that require sockets or PGA packages.

## 2 Normative references

[1] EIA/JESD51, *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)*.

[2] EIA/JESD51-1, *Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device)*.

[3] EIA/JESD51-2, *Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*.

[4] EIA/JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*.

[5] *Electronics Engineer's Handbook*, 3rd Edition, Edited by D.G. Fink and D. Christiansen, McGraw-Hill Book Co., NY, 1989, p 6.16

[6] MIL-W-5088L, Amdt. 1, *Wiring, Aerospace Vehicle*

[7] IPC-2222, *Sectional Design Standard for Rigid Organic Printed Boards*.

[8] IPC-2221, *Generic Standard on Printed Board Design*.

## 3 Stock material

The PCB test board shall be made of FR-4 material. The finish size shall be 1.60 mm +/- 10% thick. For high ambient or board temperature applications ( > 125 ºC), use of other test board material is acceptable as long as the thermal conductivity of the material is reported and measurement correlations have been established between the substitute material and FR-4.

Trace thickness is achieved by starting with standard copper finished stock and then plating to final thickness. A convention in PCB fabrication is to refer to copper thickness using the terminology of ounces of copper per square foot of board. An ounce of copper per square foot translates to a copper thickness of 35 ∝m.

The 1s test board has only a top trace layer in the component mounting and trace fan-out region (see figure 1a). The copper trace thickness shall be 70 □m (2 oz) +/- 20%. A bottom trace layer may be used for solder lands at the end of the fan-out traces and edge connection points. Connection to the edge connector outside the package fan-out region can be made with either the top or bottom signal traces. The 2s2p version of this test board is formed by embedding two 35 □m (1 oz) +0/-20% copper planes in the PCB (as shown in figure 1b), while maintaining the finished thickness at 1.60 mm.


**Figure 1a — Cross section of 1s PCB showing trace and dielectric thicknesses in package placement and trace fan-out regions**


**Figure 1b — Cross section of 2s2p PCB showing trace and dielectric thicknesses**

## 4 Board outline

The board shall be 101.5 mm x 114.5 mm +/- 0.25 mm in size for packages less than or equal to 40 mm on a side (see figure 2). A typical edge connector is depicted in figure 2. The edge connector can be pin-out and pitch modified for specific needs. Multiple rows of vias along the edge connector are allowed.

For various package sizes, refer to table 1 for the appropriate PCB size.

**Table 1 — PCB sizes for packages**

| Package Length | PCB Size (+/- 0.25 mm) |
|---|---|
| Pkg. Length ″ 40 mm | 101.5 mm x 114.5 mm (4.0" x 4.5") |
| 40 mm < Pkg. Length ″ 65 mm | 127.0 mm x 139.5 mm (5.0” x 5.5”) |
| 65 mm < Pkg. Length ″ 90 mm | 152.5 mm x 165.0 mm (6.0” x 6.5”) |

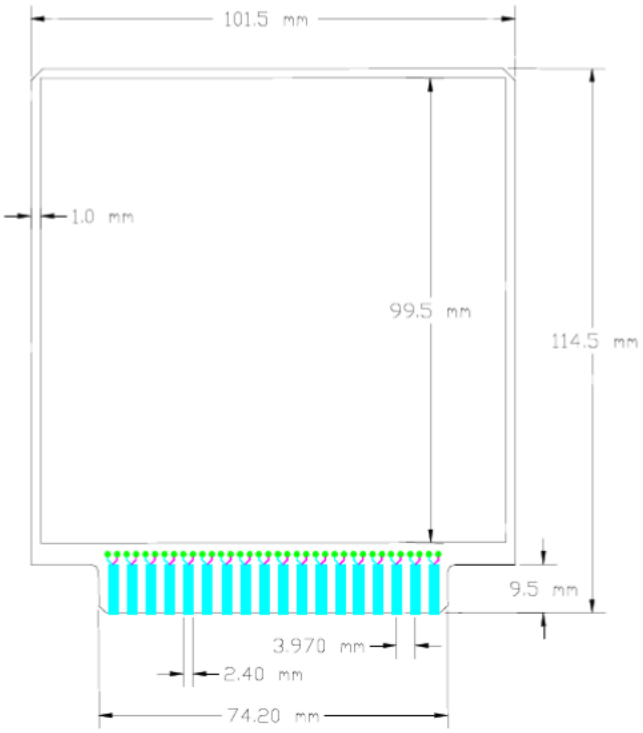



**Figure 2 — Example test board outer dimensions and edge connector design.**

## 5 Trace design

### 5.1 Top trace layer layout (both 1s and 2s2p PCBs)

Traces should be laid out such that the test device will be centered relative to a 101.5 mm x 101.5 mm section towards the top of the board (away from the edge connector) for the smallest board. For larger board sizes, locate the package at the top of the board in the center of a square whose length is the width dimension of the board. The package shall be oriented such that the long dimension of the package body is perpendicular to the edge connector. The traces connecting to the package must extend at least 25 mm out from the edge of the device body. Trace lengths longer than this are allowed. Traces must be routed in a radial fashion (flared) to meet the edges of a rectangle such that the terminal via locations are equally spaced over 90% of the perimeter of the sides of this rectangle. Traces must be flared out to the 25 mm perimeter adjacent to the side of the package on which they originate.

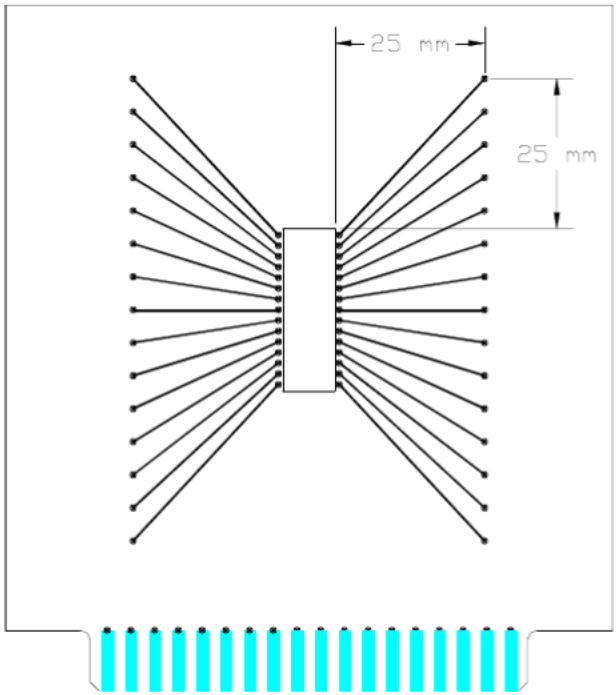



**Figure 3— Traces flared to perimeter 25 mm from package body**

A single PCB design can be used for a family of packages with the same pin pitch as long as the traces are fanned out to meet the requirements for the largest body size (see figure 4).

For packages with a single row of leads, the odd numbered pins should be fanned out to one side of the pattern and the even numbered pins should fan out to the opposing side (see figure 5)

## 5 Trace design (cont'd)

### 5.1 Top trace layer layout (both 1s and 2s2p PCBs) (cont'd)

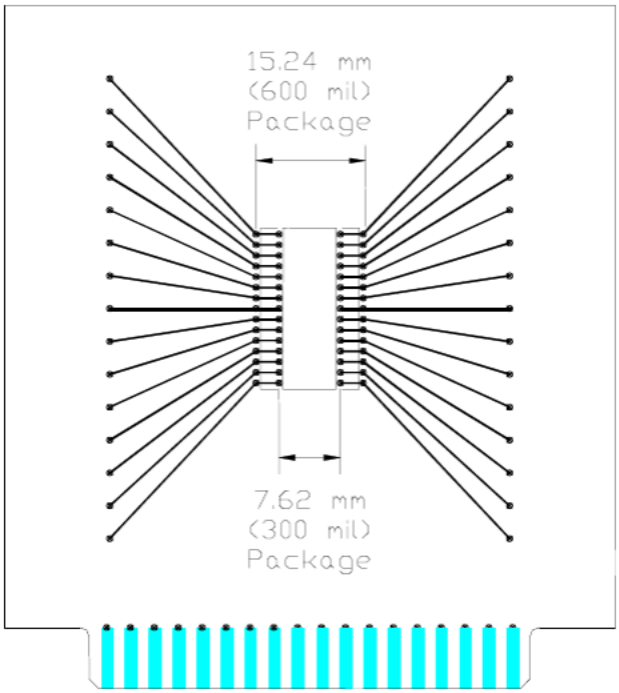



**Figure 4 — Nested design with traces flared to perimeter 25 mm from from largest package body.**

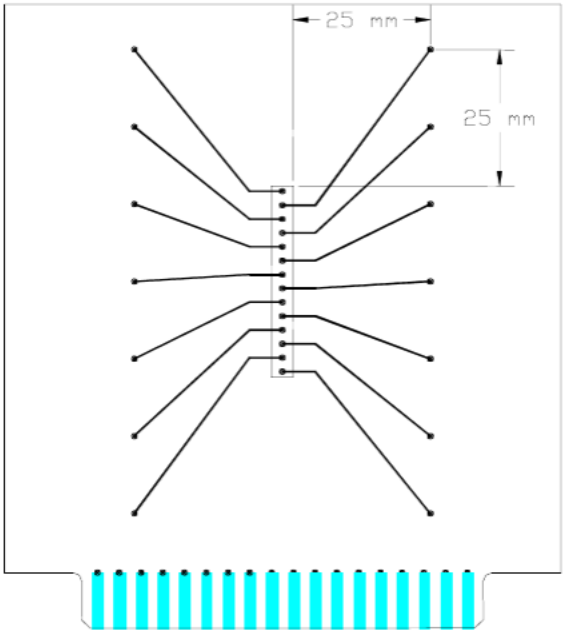



**Figure 5 — Traces flared to perimeter 25 mm from SIP body.**

## 5 Trace design (cont'd)

### 5.2 Trace widths for 1s and 2s2p PCBs

The total trace widths connecting to one package terminal shall be 0.25 mm +/- 10%. Splitting of traces in two parts, e.g. in order to keep force (power) and sense (measure) lines independent, is allows as long as their summed widths meets the above specified total trace width. Achieving the finish size may require some oversize in design to compensate for over-etching of the copper traces during processing. Traces should terminate in a plated through-hole for soldering interconnect purposes.

### 5.3 Plated through-hole vias

Vias for Package Mounting: The finished (plated) diameter for all plated through-holes used for package mounting shall be no less than the maximum pin diameter plus 0.15 mm and no more than the minimum pin diameter plus 0.60 mm [7]. For rectangular pins, the diameter shall be calculated as equal to the diagonal of the rectangular cross-section of the lead. The via pad diameter shall nominal as specified in reference [8]. The via pad diameter tolerance shall be +0.10/-0 mm.

For example, for a DIP (JEDEC MO-001, Variation AJ) with the following dimensions:

Min. lead width: 0.381 mm
Max. lead width: 0.584 mm
Nominal thickness: 0.25 mm

The lead diameters are as follows:

Min. lead diameter: 0.46 mm
Max. lead diameter: 0.64 mm

The plate through-hole vias are as follows:

Min. finished hole diameter: 0.64 + 0.15 = 0.79 mm [7]
Max. finished hole diameter: 0.46 + 0.60 = 1.06 mm [7]
Via pad diameter: 1.06 + 0.20 + 0.10 = 1.36 +0.10/-0 mm [8]

The drill hole diameter shall be such as to yield the finished hole diameters specified above. An isolation clearance region with a diameter at least 0.2 mm larger than the drill hole diameter shall exist in the buried solid planes around each plated through-hole via. Other than this isolation clearance area, the buried planes are to be unbroken. Some buried plane copper must exist between via isolation clearance regions; the clearance regions are not to merge into one another. Except for any thermal pins (see 5.4), all package mounting vias shall be isolated from any buried solid planes.

Trace fan-out vias: The plated through-hole vias at the border of the trace fan-out area and beyond shall have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter. A block out area or isolation clearance of diameter no greater than 0.70 mm larger than the drill hole diameter shall exist in the buried solid planes around each plated through-hole via. Other than this isolation clearance area, the buried planes are to be unbroken. Some buried plane copper must exist between via isolation clearance regions; the clearance regions are not to merge into one another.

## 5 Trace design (cont'd)

### 5.4 Thermal pins (2s2p only)

Pins that are directly connected to the die pad shall be connected to the top buried copper plane. These pins shall be isolated from the bottom copper plane as specified in 5.3. A cross pattern on the connected plane shall not be used; the plane shall remain unetched in the vicinity of the drill hole.

### 5.5 Trace layers and connection routing

1s PCB: The only pattern permitted within the flared perimeter (fan-out area) is the fan-out pattern and package footprint on the top trace layer. The bottom layer shall be used only for via termination and limited connection routing to the edge connector. Routing to the edge connector is allowed in either the top or bottom signal layers if the interconnection remains outside the flared perimeter of the through-holes. No traces are allowed to run under the PCB within the flared perimeter of the through-holes. Power connection routing should be designed to minimize voltage drops and self heating across the PCB traces. Measurement force (power) and sense (measure) lines should be kept independent of each other from the edge connector to the package terminals.

2s2p PCB: The top trace layer shall be used for fan-out and interconnection to the edge connector outside the fan-out perimeter. Any required interconnection routing to the edge connector can be made using the bottom trace layer and the top layer as long as the top layer interconnection remains outside the package fan-out region. Power connection routing should be designed to minimize voltage drops and self heating across the PCB traces. Measurement force (power) and sense (measure) lines should be kept independent of each other from the edge connector to the package terminals. Vias between "signal traces" and the buried planes are allowed for power and ground connections only and must be at the end of the fan-out traces.

### 5.6 Buried layer layout (2s2p PCB only)

The power and ground planes embedded in the board shall be of 0.035 mm (1 oz) copper +0/-20% . They are to be continuous except for via isolation clearance patterns. The power and ground planes shall terminate 1.0 mm from the edges of the PCB, giving overall plane dimensions as listed in table 2. The power and ground planes must not be present in the 9.25 mm edge connector pattern location shown in figure 2.

**Table 2 — PCB buried plane sizes**

| PCB Size (+/- 0.25 mm) | Buried Plane Size |
|---|---|
| 101.5 mm x 114.5 mm | 99.5 mm x 99.5 mm |
| 127.0 mm x 139.5 mm | 125.0 mm x 125.0 mm |
| 152.5 mm x 165.0 mm | 150.5 mm x 150.5 mm |

## 5 Trace design (cont'd)

### 5.7 PCB metalization characteristics for 1s and 2s2p PCBs

Top and bottom trace metalization on the PCB should be 70μm (2 oz) +/-20% finished thickness. This is achieved by starting with a 1 oz copper material and plating to 2 oz during PCB through hole plating process. This process specification should be printed on all drawings to insure proper processing. The thickness of the copper traces should be verified to +/- 20% after PCB fabrication because thickness variations greater than this can have an excessive influence on the performance of the PCB.

### 5.8 Solder masks for 1s and 2s2p PCBs

Solder masking is required and must follow the constraints described for the pads in 5.3.

## 6 Hand wiring

Connection to edge connector: Connection from the through-holes to the edge connector shall be made with 22AWG copper wire or smaller if the connections are not designed as part of the trace pattern. When the board is intended for use in forced air measurement environments, interconnect wiring to the edge connector shall be on the trailing edge of the board with respect to air flow direction and back side of the board with respect to the component placement. Interconnect wiring shall be outside the fan-out area. Figure 6 shows a suggestion for wiring from the leading edge of the test board to the trailing edge before being routed to the edge connector. Connection from the edge connector to the fan-out perimeter and from the fan-out perimeter to the power dissipation structures must be made in a four-point method for force (power) and sense (measure) purposes. Wire diameters for heating force currents may need to be larger to accommodate high power tests and may require more than one edge connector pin. Use table 3 as a guide to determine the required wire diameter [5,6].

**Table 3 — Wire size current limits**

| AWG Wire Size | UL Current Capacity, (80 ºC), Amperes | MIL-W-5088B Amperes |
|---|---|---|
| 30 | 0.4 | N/A |
| 28 | 0.6 | N/A |
| 26 | 1.0 | N/A |
| 24 | 1.6 | N/A |
| 22 | 2.5 | 5.0 |
| 20 | 4.0 | 8.3 |
| 18 | 6.0 | 15.4 |
| 16 | 10.0 | 19.4 |
| 14 | 16.0 | 31.2 |
| 12 | 26.0 | 40.0 |

**6 Hand wiring (cont'd)**

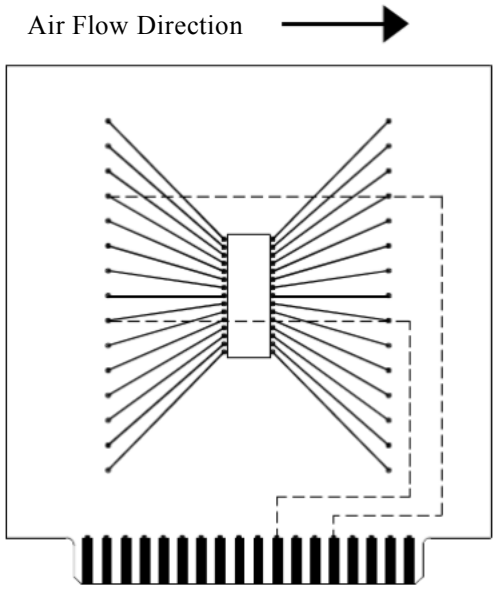


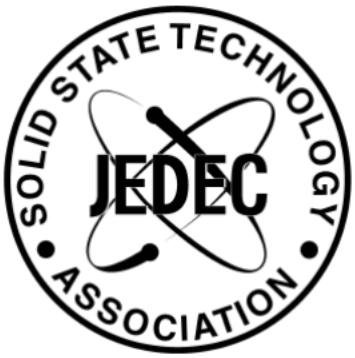

**Figure 6 — Dashed lines show hand wiring across back of test board to avoid interrupting air flow on leading edge of board for air flow measurement environments.**

## 7 Data presentation

Table 4 lists parameters specified by this document. The “user” column allows the user to input actual measured values from the test boards.

**Table 4 — Specified parameters and values used**

| | Dimension | Specification | User |
|---|---|---|---|
| 1 | Board Finish Thickness | 1.60 mm +/- 10% | |
| 2 | Board Dimension (+/- 0.25 mm) | ❑ 101.5 mm x 114.5 mm [PKG ″ 40 mm]<br>❑ 127.0 mm x 139.5 mm [40 < PKG ″ 65 mm]<br>❑ 152.5 mm x 165.0 mm [65 < PKG ″ 90 mm] | |
| 3 | Board Material | FR-4 | |
| 4 | Dielectric Layer Thickness | 0.25 mm ″ thickness ″ 0.5 mm | |
| 5 | Fan-out Trace Length from package body (minimum) | 25 mm | |
| 6 | Fan-out Trace Position | ❑ centered in 101.5 mm x 101.5 mm section [PKG ″ 40 mm]<br>❑ centered in 127.0 mm x 127.0 mm section [40 < PKG ″ 65 mm]<br>❑ centered in 152.5 mm x 152.5 mm section [65 < PKG ″ 90 mm] | |
| 7 | Copper Trace Thickness | 70 ∝m +/-20% | |
| 8 | Finished Trace Width | 0.25 mm +/-10% | |
| 9 | Trace Coverage Area (total) | | |
| 10 | Package Mount Via Finished Diameter | Minimum = maximum pin diameter + 0.15 mm<br>Maximum = minimum pin diameter + 0.60 mm | |
| 11 | Package Mount Via Pad Diameter | Nominal as specified by reference [8] | |
| 12 | Package Mount Via Isolation Clearance | Drill diameter + 0.2 mm minimum | |
| 13 | Nested? | Yes/no: package body sizes nested | |
| 14 | Backside Interconnect? | Yes/no | |
| 15 | Multi-layer (buried pwr/gnd) | Yes/no | |
| 16 | Power/Ground Thickness | 35 ∝m (1oz) copper +0/-20 % | |
| 17 | Power/Ground space to PCB edge | 1 mm | |
| 18 | Power/Ground connected to fan-out vias? | Yes/no: number of connections | |
| 19 | Solder Mask (required) | Type | |
| 20 | Number of Thermal Pins | | |
| 21 | Fan-out Trace Via Land | 1.25 mm | |
| 22 | Fan-out Trace Via Drill Hole | 0.85 mm | |
| 23 | Fan-out Trace Via Isolation Clearance | ″0.70 mm oversize of via hole; buried plane continuity assured through via regions | |
| 24 | Wire Gauge (Sense) | ″ 22 AWG | |
| 25 | Wire Gauge (Heater Force) | See Table 3 | |
| 26 | Heater sense lines merged with force lines? | ❑ on die<br>❑ in package<br>❑ on PWB | |
| 27 | TSE sense lines merged with force lines? | ❑ on die<br>❑ in package<br>❑ on PWB | |
| 28 | Drawings Available? | Yes/no | |


SOLID STATE TECHNOLOGY
JEDEC
ASSOCIATION