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## Constant Temperature Aging to Characterize Aluminum Interconnect Metallization for Stress-Induced Voiding

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# GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING

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# GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING

(From JEDEC Board ballot JCB-00-31, formulated under the cognizance of the JC-14.2 Committee on Wafer-Level Reliability.)

## 1 Scope

This document describes a constant temperature (isothermal) aging method for testing aluminum (Al) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding.

This method is valid for metallization/dielectric systems in which the dielectric is deposited onto the metallization at a temperature considerably above the intended use temperature, and above or equal to the deposition temperature of the metal.

If the metallization is a single-alloy component, such as AlSi or AlCu, the failure criterion of the method is an open-circuit of the test structure. The failure criterion for layered metallizations with refractory shunt layers (such as titanium (Ti), titanium nitride (TiN), tungsten (W), etc.) is a preselected percent increase in resistance of the test structure.

The method assumes that void growth and therefore resistance changes can be modeled, as described by Rauch and Sullivan [1, 2], to obtain an acceleration factor for void growth.

Although this is a wafer test, it is not a fast (less than 5 minutes per probe) test. It is intended to be used for lifetime prediction and failure analysis, not for production Go-NoGo lot checking.

## 2 Introduction

### 2.1 Stress-induced voids

Stress-induced voiding, which can occur during processing, storage, and use, is a reliability concern for microelectronics chips that use Al-based alloys for on-chip wiring. The subject has been extensively reviewed by Okabayashi [3]. Susceptible metallizations can grow voids in lines and under or over W studs. For simple metallizations like AlSi, such voids can cause catastrophic failure. For metallizations of Al layered with a refractory shunt layer, voids cause resistance increases and interact with other failure mechanisms, such as electromigration and mechanical failure, to shorten lifetime.

## 2 Introduction (cont'd)

### 2.2 Void growth

Once voids have nucleated, the rate of void growth is controlled primarily by two quantities: 1) the tensile stress in the Al, and 2) self diffusivity of the Al. The tensile stress increases linearly as temperature decreases below the dielectric deposition temperature, while diffusivity increases exponentially with temperature. The product of these two factors produces a peak in the rate of void growth which is located between the dielectric deposition temperature and use temperature. Published data indicates that this peak can occur anywhere in the range from 90 $^{o}$C to 300 $^{o}$C [4, 5, 6].

### 2.3 Technology-dependent factors

A variety of technology-dependent factors define and modify the stress distribution and the diffusivity in the Al. A partial list of such secondary factors includes:

- Al microstructure and alloy impurities,
- Al deposition temperature,
- prior heat treatment,
- properties of the passivation layer,
- interfacial adhesion between the passivation and Al,
- refractory cladding layers and associated mechanical properties,
- line dimensions,
- electrical properties of cladding layer,
- interfacial diffusivity ($Al/SiO_2$, $Al/TiAl_3$, etc.)
- metal-etch profile of the line in cross section,
- layout shape,
- the presence, configuration, and material of inter-level interconnects,
- passivation deposition temperature,
- cool-down rate of wafer after last process step, from temperatures comparable to the passivation deposition temperature, and
- intermetallic reactions (for layered metallizations).

### 2.4 Post processing factors

Although this document is intended to apply primarily to wafers, it should be noted that additional factors besides wafer-level processing could influence stress-voiding behavior. These include, but are not limited to, extended packaging processing and testing, card mounting processing, and system assembly.

## 2 Introduction (cont'd)

### 2.5 Void nucleation factors

Besides factors which influence void growth, an additional class of factors exist which influence void nucleation. These include several of the factors listed in 2.3. Other considerations should include the presence of etch residue contaminants or metal damage (holes, roughness, etc.) after metal etch and cleaning, line-width, ratio of grain-size to line width, and the amount of the alloying element (such as Cu) and variations in line widths and grain size distribution.

### 2.6 Structures

To test the susceptibility of the technology in question, structures which emphasize each extreme of the technology should be designed and evaluated. (See section 3.3 for more discussion.)

### 2.7 Stress temperature

To evaluate the impact of stress voiding on chip reliability under use conditions, accelerated testing is needed to generate voiding. Because the acceleration factor, which depends on stress in the Al and Al mass transport (diffusivity), can be very strongly affected by the factors listed in 2.3, the selection of the temperature for accelerated testing which will maximize voiding is not obvious in advance and must be determined empirically.

### 2.8 Void volume

Assuming the oxide behaves elastically, the maximum volume of voiding in a specific structure can be calculated by assuming that only thermal contraction of the Al is relevant. (See paragraph 4.6 in *Precautions and Interferences* for limitations on this assertion.) Then the maximum volume possible for voiding is equal to the volume change for unconstrained Al, and is given by

$$\varnothing V = 3\,\alpha * \varnothing T * V, \qquad (1)$$

where $V$ is the volume of the interconnect of concern, $\alpha$ is the thermal expansion coefficient of Al (approximately $25\times10^{-6}$ $K^{-1}$), and $\varnothing T$ is the difference in temperature between the passivation deposition temperature and the stress (bake) temperature. If the bake temperature is taken at room temperature and the passivation deposition temperature is 425 $^{o}$C, for example, then $(\varnothing V/V)max$ = 3%. Clearly, at higher use temperatures, this relative volume will be less. Observation of voiding in excess of 3% at room temperature is likely to mean that some other mechanism in addition to, or besides, stress voiding is involved.

## 3 Constant temperature aging test method

### 3.1 Constant temperature aging for stress-induced voids

The test method most likely to detect sensitivity to stress voiding and the one most usually conducted is constant temperature (isothermal) aging, i.e., annealing or baking at temperatures between the passivation deposition temperature and the intended use temperature of the product. The wafers are baked, cooled periodically to room temperature, and measured for any changes in resistance of the structures under test. Some studies have shown that cooling down wafers after the last high-temperature process (high temperature meaning comparable to passivation deposition temperature) can alter the size of the voids nucleated in the Al. However, little change in void size is expected during cooling down from the test temperature to make resistance measurements, or during subsequent reheating. (See 4.3 and 4.4 for related information.)

**3.2 Suggested procedure** (See also 3.2.8 for a decision list)

3.2.1 Select ten wafers, for example, from each of three wafer lots (a total of 30 wafers).

3.2.2 Measure sheet resistances and line resistances of relevant test structures on these wafers, as received, at wafer level for two reasons:

- to ensure that the measured resistances fall within expected ranges for the structures involved and the applicable design rules and
- to compare these resistance values with those measured during constant temperature aging.

3.2.3 Separate wafers into five groups, each group to be baked at a different temperature (e.g., 175, 200, 225, 250, and 275 °C), such that each group contains two wafers from each of the three lots (or a total of six wafers). (If the temperature for peak voiding is not known for the metallization under test, additional temperatures up to the passivation deposition temperature may be needed.)

3.2.4 Bake (thermally age) the wafers at the specified temperatures and cool in less than 2hrs to room temperature (see precautions in 4.4 and 4.5 on rate of temperature change) for test readouts (e.g., at 24, 48, 100, 250, 500, 750, 1000, 1500, and 2000 h). At each test readout, re-measure the resistances of each of the structures measured before continuing to bake.

3.2.5 Report failures for each readout for each structure. Failure is defined by a predetermined resistance increase (e.g., 5%). Plot cumulative failures vs. the log of readout time, assuming failure times are log-normally distributed.

**3 Constant temperature aging test method (cont'd)**

**3.2 Suggested procedure (cont'd)**

3.2.6 Count the number of voids in stressed parts (from scanning electron microscope (SEM) photos of delayered mazes) to determine void nucleation density in structures of interest, if the void density is relevant to the chip design.

3.2.7 Determine the lifetime (3.5.5). Optionally, use the acceleration factor (3.5.6) to determine the lifetime at use conditions from the accelerated stress data.

3.2.8 Procedures to be agreed upon before starting (Procedures Summary)

| Description | Ref. Paragraph |
|---|---|
| Define Bake Temperatures | 3.2.3, 3.4.2 |
| Define Measurement Intervals (test points) | 3.2.4, 3.4.3 |
| Define Failure Criteria (fractional % R change) | 3.2.5 |
| Define Lot and Replication Samples (wafer samples, n-samples/wafer, etc.) | 3.2.1, 3.4.2 |
| Define Structure | |
| Line Configuration (straight, surpentine, W-studs. . .) | |
| Width or (line-width/grainsize) ratio | 3.3.3 |
| Line Length | 3.3.1, 3.3.2 |
| Stud Size & Placement | 3.3.4 |

**3.3 Test structures**

3.3.1 Several different types of structure have been observed to be sensitive to stress voiding. Long narrow lines (centimeters to meters in length), shorter narrow lines (approximately 1 mm long), and lines with overlying and underlying W studs are examples. Often, structures having several narrow widths are required due to variation in nucleation densities related to Al microstructure (e.g., the density of grain boundary triple points). Narrow lines are important because the stress in the Al is typically higher in narrower lines than in wider lines. But, depending on the minimum ground rule dimensions and the grain size of the metallization, the line with minimum width may not be the most susceptible to voiding; hence the advised distribution of widths.

3.3.2 Long, narrow lines (serpentines, mazes) provide sufficient length to insure that void nucleation sites will exist, and will produce voids if the metallization/insulator system is susceptible. The change in resistance with time at stress temperature of such structures provides a good measure of the relative average void density in the line.

## 3 Constant temperature aging test method (cont'd)

### 3.3 Test structures (cont'd)

3.3.2.1 However, if the narrowest lines are primarily bamboo in structure, the void density may be lower than for wider lines and the corresponding resistance increase will be smaller. In this case, shorter lines are useful because they will manifest a higher fractional change in resistance when voiding is present. However, fewer of them will register any resistance shift at all because of the spatial distribution in nucleation sites.

3.3.2.2 In addition, stress voiding in these structures is often sensitive to line-to-line separation in the maze; therefore, single, long, isolated lines should also be available. The line-to-line separation sensitivity can be caused by several factors, among which are:

- line width variations caused by variations in etching with metal density,
- variations in oxide density due to interline aspect ratio and fill, and
- additional lateral stress arising from the presence of neighboring metal.

3.3.3 Multiple line widths are needed to evaluate sensitivity to the ratio of grain-size to line-width. These widths can be 1.1, 1.3, and 2.0 times the minimum line width or the average grain size.

3.3.4 For multi-level metallizations, structures having W-studs underlying and/or overlying the line structures are effective because W has a larger thermal expansion coefficient than $SiO_2$. Hence, the stress in Al lines immediately above or below the studs is greater than elsewhere in the line. When a nucleation site is located under or over a stud, the incidence of void nucleation is often elevated. In the case of overlying and underlying W studs, the volume of the Al interconnect attached to the stud must be sufficient to generate a void large enough to extend beyond the stud. Otherwise, it will be difficult to detect electrically the presence of the void. *(∅V/V)max* can be calculated by Eq. 1 in 2.8 (also, see paragraph 4.6 under *Precautions and interferences* for limitations on Eq. 1).

### 3.4 Test conditions, procedures, and measurements

3.4.1 Stress voiding can vary significantly within a single wafer, such that for a specific structure, some regions of the wafer will show no voiding, while other regions may exhibit very extensive voiding. Also, the distribution across the wafer of chips showing voiding often varies from wafer to wafer. Thus, depending on the pattern of chips picked from a wafer, detection of stress voiding at the chip level may be obscured. In addition, testing of chips or packages requires more processing and is more time consuming than for wafers. Hence, both for testing practicality and statistical reasons, wafer testing rather than chip or package testing is advisable.

**3 Constant temperature aging test method (cont'd)**

**3.4 Test conditions, procedures, and measurements (cont'd)**

3.4.2 As stated in 2.2, the product of the diffusivity and the stress in the Al determines the peak temperature of voiding. The diffusivity derives from the mass transport properties of the Al and the impact of line width, for example. The stress in the Al depends primarily on the passivation deposition temperature and the Al deposition temperature. These factors will vary with the technology and the tool set. To determine the peak temperature of void growth, several temperatures below the oxide deposition temperature should be employed. A typical spread might be 175, 200, 225, 250, 275 $^{o}$C, depending on the fabrication processes involved. However, when no prior experience exists, additional temperatures down to 100 $^{o}$C and up to the passivation deposition temperature would be advisable (e.g., 100, 125, and 150 $^{o}$C, and 300, 325, 350 and 375 $^{o}$C). One wafer per temperature from each of several lots is needed to account for lot-to-lot variation. For more information on temperature of peak voiding, see references [3,4,5,6].

3.4.3 Resistance measurements may extend beyond 2000 h if saturation of void growth is desired. Saturation in void growth, and hence saturation in resistance change, can be used to estimate the level of maximum strain initially present in the Al [2] If resistance shifts and void size have been correlated through failure analysis, void density can also be obtained [2]. Early measurements should be relatively frequent to capture rapid, initial resistance changes, which may occur as the result of irregular void shape. The frequency at later times can be reduced to limit the amount of data storage required. A typical readout schedule might be 0, 24, 48, 100, 250, 500, 1000, 1500 and 2000 h. The onset of resistance changes occurs more quickly for narrower lines, which may shorten the test if detection of voids is the sole purpose.

**3.5 Data interpretation**

3.5.1 There are several ways to interpret the data. The most straightforward one uses a procedure similar to that used for electromigration and employs the median time to failure, where failure is determined by either a specified resistance shift or an open circuit. In this context, it should be noted that a wedge shaped void growing across a line would cause an open circuit in a simple metallization like AlSi at the same volume as it has when causing the first significant resistance shift in a layered metallization. Therefore, a rough equivalence exists between the first measured resistance shift in a layered metallization and the first open in a simple metallization.

**3 Constant temperature aging test method (cont'd)**

**3.5 Data interpretation (cont'd)**

3.5.2 In attempting to compare voiding data from one company to another, care must be used to allow for differences in the effective sheet resistances of the cladding layers. The resistance shift produced by a 1 µm long void in a line that is 1 µm wide will be determined by the resistivity and thickness of the cladding layer in the voided region. The thicker the layer, the smaller the resistance change. A Ti layer will produce a greater resistance change than a W layer of the same thickness because of the higher resistivity of the Ti. In addition, the Ti layer made by one tool is likely to differ in resistivity from that made by another tool, due to impurity incorporation, for example.

3.5.3 Because extended duration may be required to produce sizeable resistance shifts, a lower relative resistance failure criterion may be desired. For example, median time to a 1% resistance shift would be substantially shorter than for a 20% resistance shift.

3.5.4 The time-to-failure for the chosen fractional change in resistance is found either from plots of the fractional resistance change versus 1) stress time, or 2) square root of stress time. Void growth is generally agreed to be a diffusive process and the increase in line resistance (for layered metallizations) is proportional to the void length, which should be proportional to a diffusion length. Thus a plot of fractional resistance change versus the square root of the time has the advantage of being approximately linear until void growth approaches saturation. Failure time is recorded when the resistance exceeds the level defined for failure.

3.5.5 A physical model [1, 2], similar to Black's Law for electromigration, can be used to relate the failure time to physical variables and is given by

$$t_f = A * (1/\varnothing T^2) * \exp(\varnothing h/kT) , \qquad (2)$$

where $t_f$ is the median time to failure, $A$ is a constant, $\varnothing T$ is as defined for Eq. 1, $\varnothing h$ is the effective activation energy for the diffusion process, $k$ is Boltzmann's constant, and $T$ is the stress temperature.

## 3 Constant temperature aging test method (cont'd)

### 3.5 Data interpretation (cont'd)

3.5.6 An effective acceleration factor for stress voiding can be obtained from the ratio of the failure time under use conditions to that under stress conditions, and is given by

$$AF = t_{fu}/t_{fs} = (\varnothing T_s/\varnothing T_u)^2 * exp\,[(\varnothing h/k) * (1/T_u - 1/T_s)], \qquad (3)$$

where the subscripts *u* and *s* denote use and stress conditions, respectively. Assuming the oxide to be rigid and the metal fully expanded at the passivation deposition temperature (this is not usually the case -- see paragraph 4.7 under PRECAUTIONS AND INTERFERENCES for possible pitfalls in using this equation), the only unknown in Eq. 3 is the effective activation energy. This can be obtained from a plot of $t_f$ versus $1/(k*T)$ for several temperatures. The effective activation energy is influenced by the stress in the Al, by the microstructure of the line within several tens of microns on either side of the void, and by contributions to mass transport from interfacial diffusion. Care should be taken when using Eq. 3 that void growth has not saturated. For this reason, low percentage resistance shifts (5%, for example) are recommended for use as the failure criterion when attempting to determine the effective acceleration factor or the effective activation energy.

3.5.7 Activation energy is a controversial quantity in stress voiding. However, from an empirical perspective and with respect to the acceleration factor given in Eq. 3, an effective activation energy can be defined and used. Two different methods can be employed. In the first method, the maximum or average resistance shifts for large numbers of structures of the same type baked at different temperatures can be fit by the model of Rauch and Sullivan [1, 2] to produce the activation energy. In the second method, the median time to failure obtained for the same structure at several temperatures can be plotted against $1/kT$ and the resulting slope is interpreted as the effective activation energy. Difficulties in interpreting data in this way can be encountered in AlCu alloys because the Cu precipitation changes with temperature due to the change in solubility.

## 4 Precautions and interferences

### 4.1 Variation of resistance change

In many cases, not all structures on a wafer will exhibit resistance shifts. This may be due to several causes, such as across-wafer variation in line width, across-wafer variation in temperature during oxide deposition, metal thickness variation, etc. If all wafers are similar in behavior and the wafer map pattern of resistance shifts is also the same, this can be handled by considering only the failing structures. However, if failure is random and varies from wafer to wafer as well, more sophisticated techniques for analysis will likely be required.

## 4 Precautions and interferences (cont'd)

### 4.2 Copper solubility

In the case of AlCu alloys, interpretation of the data needs to be done with awareness that the Cu solubility changes over the range of temperatures of interest and may affect the results. For example, 0.5% Cu dissolves completely in the Al at 310 $^{o}$C, which may change the mass transport above this temperature.

### 4.3 Comparisions

Comparisons of voiding behavior between different Al alloys should always be done with caution. Differences in both the concentration and type of solute element produce enormous differences in voiding behavior. For example, voiding in AlCu alloys containing Si in the range from 0.6% to 6% is roughly proportional to the Si concentration.

### 4.4 Thermal cycling

Thermal cycling of wafers has been reported as a means for detecting metal susceptibility to stress voiding. The user should be aware that the cooling rate can have a very strong influence on the rate of void growth and the effect may vary from one metallization to another. While thermal cycling may produce voids, the modeling of the growth rate is more complex, and the amplitude and absolute values of the thermal cycle limits may influence nucleation.

### 4.5 Peak temperature

Problems can be encountered when thermal cycles with peak temperatures in excess of the peak temperature of voiding are employed. This is because the voided metal is driven into a compressive state in which healing (void filling) occurs at the high temperature, and void growth occurs at the lower temperatures. Healing, rather than voiding would be promoted by such conditions.

### 4.6 In situ measurements

Measurement of the resistance changes is, in principle, possible in situ at the aging temperature. However, due to the long duration of the test and the fact that it is conducted at wafer level of fabrication, considerable investment in oven electronics is required. Wafer probing at the temperatures used is impractical and thermal control is difficult. In addition, the measurement must account for the thermal coefficient of resistance for both the Al and the refractory shunt layer when estimating void volumes from resistance.

**4 Precautions and interferences (cont'd)**

**4.7 Calculated void volume**

For several reasons, Eq. 1 is generally an overestimate of the maximum volume of voiding. First, the temperature delta is taken as the difference between the passivation deposition temperature and the bake temperature, implying that that the enclosing dielectric is rigid, and that the metal is unconstrained and allowed to expand freely until encapsulated in the oxide. Neither of these cases is accurate. The metal is constrained by the substrate and therefore does not expand to its full potential, and the oxide relaxes somewhat in response to the tensile stress in the Al at temperatures below the oxide deposition temperature. Both of these factors reduce the strain in the Al compared to what is predicted by Eq. 1. The result is equivalent to having a lower value for the passivation temperature in Eq. 1. Second, rather than the coefficient of thermal expansion (CTE) for Al, the difference between the CTE of Al and the surrounding oxide should be used, to be strictly accurate. (However, since the CTE for $SiO_2$ is around 0.5 parts per million (ppm), and that of Al is around 25 ppm, the error is small.) This will further reduce the magnitude of voiding predicted by Eq. 1. Since bake temperatures are generally much higher than room temperature, realistic volume fractions of voiding may be closer to 1% than 3%.

**4.8 Passivation deposition temperature**

In Eq. 3, $\varnothing T_s = T_o - T_s$, and $\varnothing T_u = T_o - T_u$, where $T_o$ is given as the passivation deposition temperature. However, as indicated above in paragraph 4.6, $T_o$ is really an "effective" passivation deposition temperature, and is likely to be less than the actual passivation deposition temperature [7] If the difference between $T_o$ and $T_{dep}$ is large, as it may be in the case of wide lines, then the value of the *AF* calculated by Eq. 3 can be significantly affected. This is easily seen by plotting the *AF* in Eq. 3 vs $T_s$ for $T_u$ = 20 °C, an activation energy of 0.5 eV, for example, and for three different values of $T_o$, 400 °C, 350 °C, and 300 °C. The corresponding peak values for the *AF* range from over 1100 to just below 300. For this reason, it is recommended that a wide enough range of temperatures be used to define the location of the peak AF and to determine the effective $T_o$.

**4.9 Joule heating**

Resistance measurements should be made at currents that minimize joule heating.

## 5 Data to be reported

| Description | Ref. Paragraph |
|---|---|
| Bake Temperatures | 3.2.3, 3.4.2 |
| Measurement Intervals (test points) | 3.2.4, 3.4.3 |
| Failure Criteria (fractional % R change) | 3.2.5 |
| Lot and Replication Samples (wafer samples) | 3.2.1, 3.4.2 |
| Structure | |
| Line Configuration (straight, surpentine, W-studs. . .) | |
| Width or (line-width/grainsize) ratio | 3.3.3 |
| Line Length | 3.3.1, 3.3.2 |
| Stud Size & Placement | 3.3.4 |
| Ro (mean, stdv, min., max.) for each stress group (t = 0h) | |
| R (mean, stdv, min., max.) each stress group, each test point. (t > 0h) | |
| Plot of the fractional resistance change versus **stress time**, for each stress group, including determined MTF.<br>-OR-<br>Plot of the fractional resistance change versus the **square root of stress time**, for each stress group, including determined MTF. | 3.5.4 |
| Plot of MTF versus 1/KT, including effective activation energy ($\varnothing h$) (if determined). | 3.5.6 |
| Lifetime at use temperature (if optionally determined). | 3.5.5 - 3.5.7 |

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