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Thermal Test Chip Guideline (Wire Bond Type Chip)

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1 Introduction

(From JEDEC Council Ballot JCB-96-25 formulated under the cognizance of JC-15.1 Committee on Thermal Characterization).

1.1 Purpose

The purpose of this document is to provide a design guideline for thermal test chips used for integrated circuit (IC) package thermal characterization. The intent of this guideline is to minimize the differences in data gathered due to nonstandard test chips.

1.2 Scope

The thermal test chips described in this document will apply to single and multiple chip devices. These are designs using standard semiconductor wafer fabrication processes and can be used with a wide variety of industry standard packages. These test chips can operate in a static mode in which constant power is continuously supplied to the device while monitoring the temperature through the measurement of a Temperature Sensitive Parameter (TSP). They can also operate in a transient mode in which the power supply and the TSP are monitored as a function of time (t). This guideline covers test chips meant to be wire bonded to the package external leads.

1.3 Rationale

The thermal resistance for a specific device varies with many factors. The chip size, location and size of the power dissipation device(s), and location of the temperature sensor(s) will directly affect the thermal test results. It is essential to standardize thermal test chip design guideline in order to provide meaningful measurement results. This allows semiconductor suppliers to compare different packages over a wide variety of conditions, such as power levels and air flows. It will also help the users to estimate their active device junction temperature under actual operating conditions by allowing them to extrapolate the results of a defined standard condition.

1.4 References

This document contains the guideline for thermal test chip design as a subset of JEDEC methodology for component package thermal measurement. The associated details of test method, environment and test board are given in JEDEC documents [1] - [4]. It is also recommended to read the SEMI test standards ([5] - [9]) and the related documents [10] - [12].

[1] JESD 51
Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)

[2] JESD 51-1
Integrated Circuit Thermal Measurement Method - Electrical Test Method (Refer to Annex A for a list of terminology and symbols applicable to this document).

[3] JESD 51-2
Integrated Circuit Thermal Test Method, Environmental Conditions - Natural Convection

[4] JC-15-95-63
Low Thermal Conductivity Test Board for Leaded Surface Mount Packages.

[5] SEMI Test Method #G43-87
Test Method, Junction-To-Case Thermal Resistance Measurements of Molded Plastic Packages.

[6] SEMI Test Method #G38-87
Still and Forced Air-to-Ambient Thermal Resistance Measurements of Integrated Circuit Packages.

[7] SEMI Test Method #G42-88
Specification, Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages.

[8] SEMI Test Method #G30-88
Junction-to-Case Thermal Resistance Measurements of Ceramic Packages.

[9] SEMI Test Method #G32-86
SEMI Guideline for Unencapsulated Thermal Test Chip.

[10] EIA JEDEC EB-20
Accepted Practices for Making Microelectronics Device Thermal Characteristics Test.

[11] Mil Std 883C Method 1012.1
Thermal Characteristics of Microelectronics Devices,

[12] NIST Special Publication 400-86
Semiconductor Measurement Technology: Thermal Resistance Measurements.

2 Test Chip Design

The thermal test chip should be designed to provide uniform heating across the chip surface, and chip temperature sensing. The general design and construction of the thermal test chip includes these basic features: heating source, temperature sensor, and bonding pads. The components of a test chip are discussed below.

2.1 Heating Source

Resistor elements or transistors should be used as heating sources. The heating power is calculated as follows:

$$P_H = V_H \times I_H \text{ (W)} \quad (1)$$

where V_H = voltage across the heating source (V)
I= current for the heating source (A)

When resistor heating is utilized, the resistance temperature dependence has to be considered in order to set the power supply. Hence, the predefined heating power is achieved by adjusting either V_H or I_H and monitoring the other because they are dependent on each other. When a transistor is used, both V_H and I_H can be adjusted separately. Therefore, the heater power dissipation is easy to control. For this reason a transistor is preferred in transient applications and when tight control of power levels is required. However, it is difficult to obtain uniform power distribution with a large transistor. Hence, for a large single unit test chip, the resistor option is preferred.

2.2 Temperature Sensor

The temperature sensing elements should function at the operating temperature range of the device. The most commonly used TSP is the voltage drop across a forward biased PN diode. This diode is specifically designed into the thermal test chip. It exhibits a linear forward voltage characteristic with temperature when a fixed measurement current (I_M) is forced through the diode. The temperature rise of most diodes is approximately 0.5 °C for 1 millivolt drop in forward voltage, that is -0.5 °C/mV. This parameter is called the K-Factor. It is process-dependent and must be determined by measuring the voltage of the diode at various temperatures. A typical diode characteristic curve is shown in figure 1. The chip temperature change can be obtained from the voltage drop with respect to a reference (usually zero power) state [2]. Another type of TSP is a Resistance Temperature Detector (RTD), which is a single metal trace. The advantage of resistance type sensors is that they are much more linear than diodes over a much wider temperature range. For a proper local measurement, the RTD may be built as a small spiral or zig-zag patch in the locations on the chip where temperature measurements are to be made. A 4-wire (Kelvin) type electrical connection must be used with RTD sensors.

2.3 Bonding Pads

The interconnect between the test chip and the package external leads is through wire bonding. The bonding pads are obtained through the standard wafer fabrication process.

2.4 Physical Layout

The basic chip unit containing the heating source(s) and temperature sensor(s) can be utilized as a single unit chips. The chip units can also be arrayed to form larger multiple unit chip. The single unit chip will generate heat uniformly. The multiple unit option gives the flexibility to generate heat uniformly if the basic units are electrically interconnected, or non-uniformly if the units are not interconnected. Interconnection between the basic units can be achieved by wire bonding or by adding metal traces during the fabrication process. If metal traces are added between units, care must be taken to ensure an adequate coverage of oxide in the scribe line to avoid shorting the interconnection traces to the substrate. Example layouts for single and multiple unit chips are shown in figures 2 and 3, respectively. Recommendations

for chip size, heating source area coverage, and temperature sensor placement are given in the following sections.

2.4.1 Chip Dimensions

Both test chip size and thickness affect the measurement data. Square and rectangular chips can be obtained using either single or multiple units configuration. The preferred sizes for newly designed test chips are listed in table 1. The use of other chip sizes is acceptable. The chip thickness used should be consistent for the same package. For each set of measurements, the thickness is determined based on the package being tested. The preferred values are 0.28, 0.375 and 0.62 mm. The use of other chip thicknesses is acceptable.

These preferred dimensions will provide sufficient choice to fit in most packages and simulate the active devices. The objective is to minimize the measurement data discrepancy due to using arbitrary test chip dimensions. When applicable, chip dimensions should be selected such that they most closely match the active device.

Table 1. Preferred chip dimensions.

Square Chip (mm^2)	Rectangular chip (mm^2)
2x2	2x4
3x3	
4x4	4x6
6x6	6x12
9x9	9x18
12X12	12x18
	12x24
15X15	
18X18	18x24
24x24	

2.4.2 Heating Source Area Coverage

The outline of the heating source should cover at least 85% of the chip area inside the bonding pads. If a multiple unit chip is utilized, each individual unit should meet this area coverage requirement. The heating elements shall be designed to dissipate power at the proper levels and provide uniform heat dissipation per unit area. Sufficient heater bonding pads shall be provided to handle anticipated current levels

2.4.3 Temperature Sensor Placement

The temperature sensors should be optimally placed to accurately measure the maximum chip temperature. When uniform heating is applied, the maximum chip temperature is at the center of the chip active surface. Therefore, in the case of single unit chip, one temperature sensor must be located at the center of the chip surface. Additional sensors may be placed in a comer and in the middle of an edge for other purposes. When a multiple unit chip is utilized, one temperature sensor should be placed at each unit center. It is also recommended that a temperature sensor be placed in a comer to provide a centrally located sensor if an even array of basic units is used. When possible each temperature sensor should be connected to four pads for forcing and sensing circuit measurement technique.

2.4.4 Wire Bonding Consideration

The recommended bonding pad sizes shall be no smaller than 0.10 mm (4 mils). The wiring for the temperature sensor and heaters shall not be connected to common bonding pads. In the case of multiple unit cells without metal interconnect traces, wire bonding to the outer cells is possible; however, bonding to the inner cells becomes increasingly more difficult as the array of cells increases in size. Therefore, it is recommended to duplicate the bonding pads and place them on two opposite sides (see figure 2). This will make wire bonding easier for a multiple unit chip because there will be at least one row of pads along the chip edge. It is also recommended that additional bonding pads be used to fully populate the perimeter of the chip. These bonding pads can then be connected to the chip package to simulate a typical application.

2.5 Surface Properties

The top surface passivation and bottom surface finish and metalization should approximate those present in package assembly process. These surfaces should have a level of adhesion between the die and adjoining materials similar to that of the application die. Failure to do so could result in different levels of delamination at the die interfaces, potentially leading to significantly different thermal performance for test and application dice.

3 Data Presentation

The test data presentation should include both thermal parameter data and test conditions. The necessary data are listed in table 2.

Table 2. Thermal measurement test conditions and data parameter summary.

Measurement Area	**Condition Parameter (s)**	**Data Parameter (s)**
Electrical	Refer to appropriate document	Refer to appropriate document
Environmental	Refer to appropriate document	Refer to appropriate document
Component Mounting	Refer to appropriate document	Refer to appropriate document
Device Construction	**Chip name & number** **Chip material** **Chip size** **Chip thickness** **Temperature sensor type** **Heating element type** **Heating source area coverage %** **Recommended I range** **Die plot (pinout)** **Top-side surface description** **Bottom-side surface description**	**K - Factor** (ref. [2] sec. 3.3)
For Single Unit Chip	**Temperature sensor location**	
For Multiple Unit Chip	**Base chip unit size** **Array topography** **Powered up units** **Temperature sensor locations**	

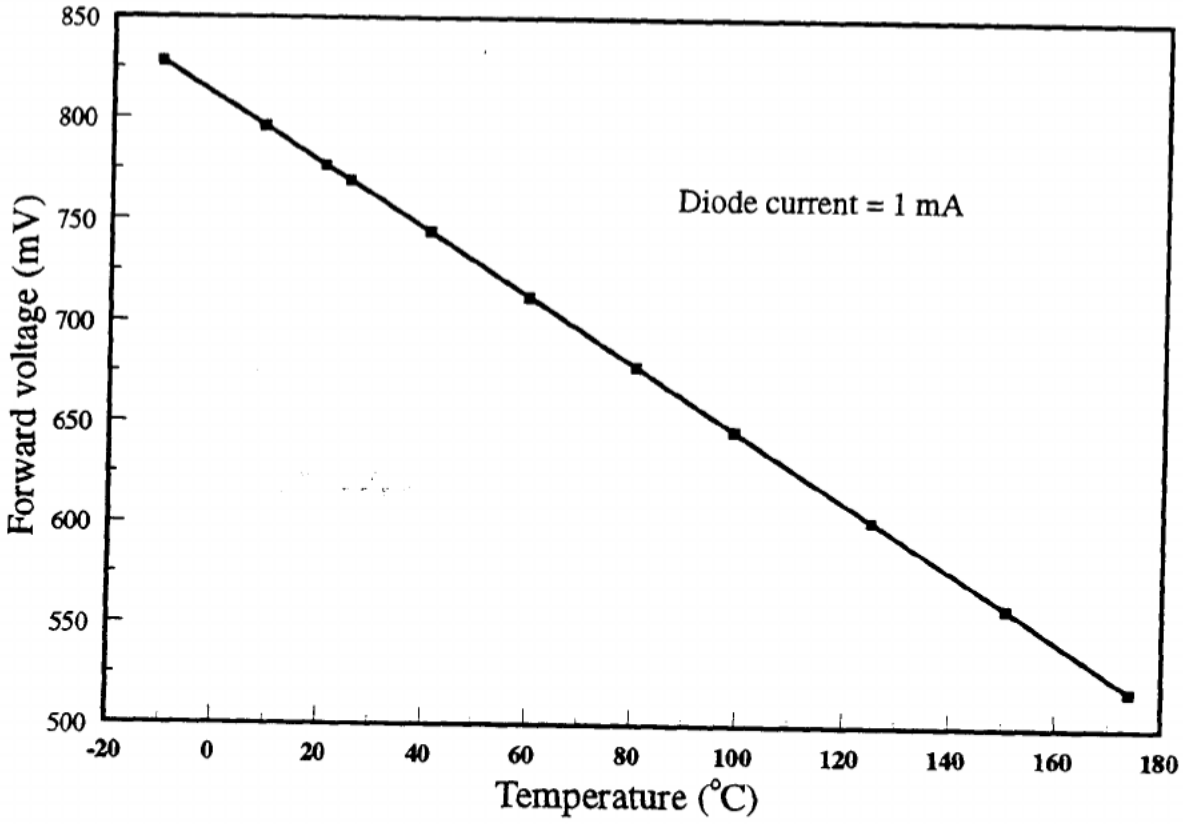

Figure 1. Typical temperature sensing diode calibration curve.

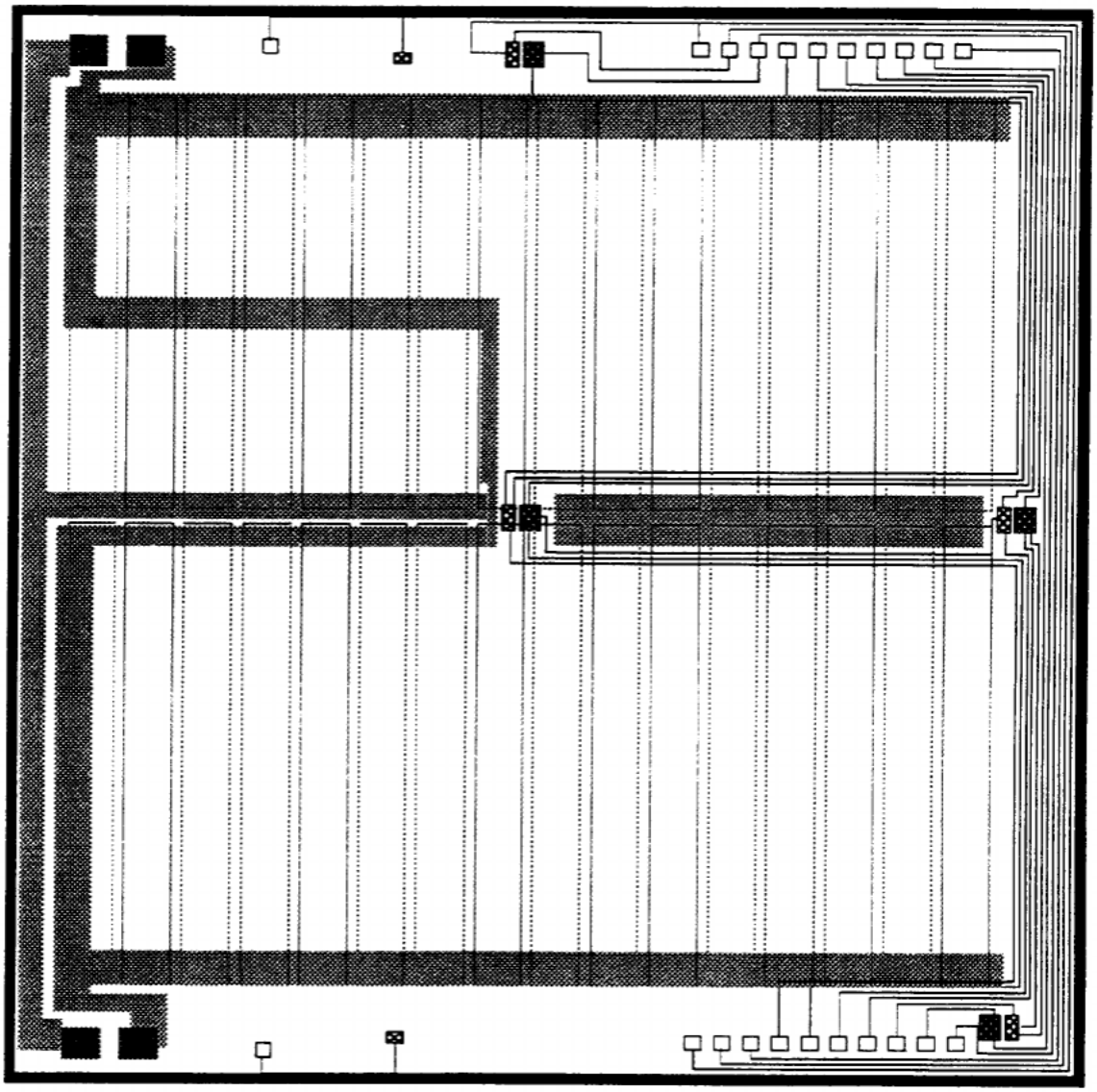

Figure 2. Single unit test chip layout (not to scale).

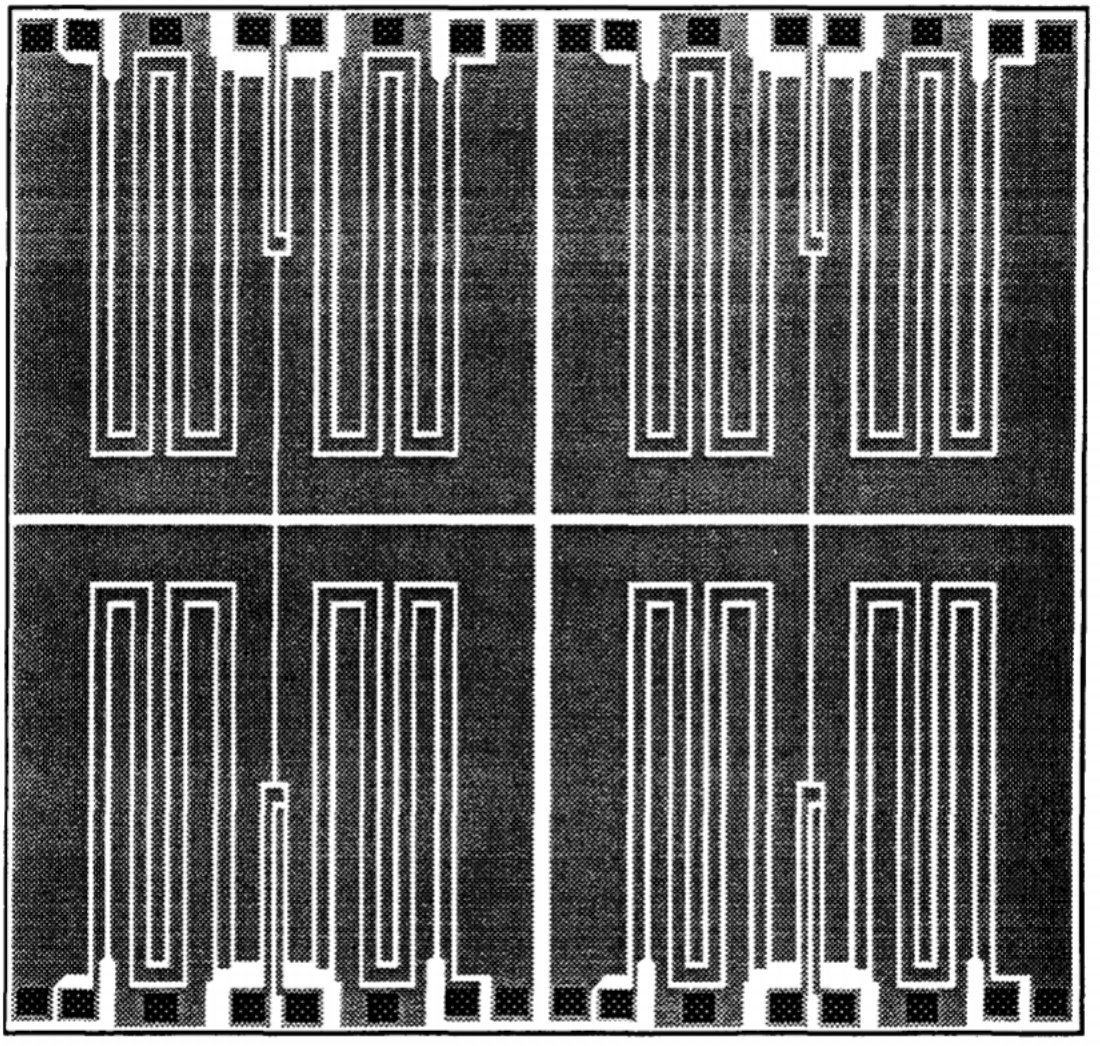

Figure 3. Multiple unit test chip layout (not to scale).